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(54) Title: METHOD OF ETCHING PATTERNED LAYERS USEFUL AS MASKING DURING SUBSEQUENT ETCHING OR FOR DAMASCENE STRUCTURES <div data-bbox="602 1220 937 1509" data-label="Image"> </div>		
(57) Abstract <p>A first embodiment of the present invention pertains to a method of patterning a semiconductor device conductive feature while permitting easy removal of any residual masking layer which remains after completion of the etching process. A multi-layered masking structure is used which includes a layer of high-temperature organic-based masking material (220) overlaid by either a patterned layer of inorganic masking material (222) or by a layer of patterned high-temperature imageable organic masking material. The inorganic masking material is used to transfer a pattern to the high-temperature organic-based masking material and is then removed. The high-temperature organic-based masking material is used to transfer the pattern and then may be removed if desired. This method is also useful in the pattern etching of aluminum, even though aluminum can be etched at lower temperatures. A second embodiment of the present invention pertains to a specialized etch chemistry useful in the patterning of organic polymeric layers such as low k dielectrics, or other organic polymeric interfacial layers. This etch chemistry is useful for mask opening during the etch of a conductive layer or is useful in etching damascene structures where a metal fill layer is applied over the surface of a patterned organic-based dielectric layer. The etch chemistry provides for the use of etchant plasma species which minimize oxygen, fluorine, chlorine, and bromine content.</p>		

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1 METHOD OF ETCHING PATTERNED LAYERS USEFUL AS MASKING
2 DURING SUBSEQUENT ETCHING OR FOR DAMASCENE STRUCTURES

3 **BACKGROUND OF THE INVENTION**

4 1. Field of the Invention

5 The present invention pertains to a method for etching of patterned layers. The
6 method is useful in high temperature etch processes where the layers are high
7 temperature masking materials or are metal-comprising layers such as copper, platinum,
8 iridium, and barium strontium titanate. The method is also useful in lower temperature
9 etch processes in which organic polymeric layers, such as low k dielectrics, are etched to
10 form damascene process structures. The present method may also be used for lower
11 temperature etching of metal layers such as aluminum or tungsten, when the pattern
12 geometry is small (less than about 0.25 μm) and etch selectivity is a problem.

13 2. Brief Description of the Background Art

14 In the field of semiconductor device fabrication, particularly with the continuing
15 trend toward smaller device feature sizes, the etch processes which are used to construct
16 conductive features such as metal interconnects and contacts have become particularly
17 critical. The new devices, having feature sizes in the range of about 0.25 μm and
18 smaller, place an emphasis on both the precise profile achievable during pattern etching
19 and on the avoidance of any residue remaining after etch which causes problems during
20 subsequent processing or problems in long term device function.

21 We previously worked to develop a plasma etching system which reduces and
22 avoids the formation of residue on the surface of a copper layer during pattern etching of
23 the copper. The etching systems useful in etching of the conductive material are
24 described in copending application Serial Nos. 08/891,410, filed July 9, 1997, and
25 08/911,878, filed August 13, 1997, both of which are hereby incorporated by reference
26 and both of which are assigned to the assignee of the present application.

1 We have simultaneously been working to develop an etching process which
2 permits the development of patterning masks which can transfer a desired pattern to
3 adjacent layers in a manner which reduces or avoids the formation of mask residue on the
4 etched structure. Further, we have worked to develop an etching process useful in
5 etching organic polymeric materials for damascene processes, where the conductive layer
6 is applied over the patterned surface of a dielectric layer to form desired conductive
7 interconnect and contact structures.

8 Figures 1A - 1E show a schematic cross-sectional view of a typical plasma etch
9 stack for etching a metal-comprising layer at temperatures in excess of about 150 °C as it
10 progresses through a series of steps including the etching of both dielectric and
11 conductive layers. This etch stack is of the kind known and used prior to the present
12 invention. Figure 1 A shows a complete etch stack, including, from bottom to top,
13 Substrate 102, which is typically a dielectric layer overlying a semiconductor substrate
14 (such as a silicon wafer substrate) or which may be the semiconductor material itself,
15 depending on the location on a given device surface. Barrier layer 104, which prevents
16 the diffusion and/or migration of material between conductive layer 106 and substrate
17 102; conductive layer 106, which is typically aluminum or copper, but might be tungsten,
18 platinum, or iridium, for example. Anti-reflective-coating (ARC) layer 108, which is
19 typically a metal-containing compound and which enables better imaging of an overlying
20 patterning layer. Pattern masking layer 110, which is typically a layer of silicon dioxide
21 or similar inorganic material which can withstand the high temperatures encountered
22 during etching of conductive layer 106, and which can be patterned and used as a mask
23 during such etching. And, photoresist layer 112 which is typically an organic-based
24 material which is stable at low temperatures and which is used to pattern masking layer
25 100, which is stable at higher temperatures. In Figure 1A, photoresist layer 112 has
26 already been patterned to provide the feature shape desired to be transferred to pattern
27 masking layer 100.

28 Figure 1B shows the stack described in Figure 1A, where the pattern in

1 photoresist layer 112 has been transferred to pattern masking layer 110, using a standard
2 plasma etching technique. When masking layer 110 comprises a silicon-containing
3 material, such as silicon dioxide, the etch plasma typically comprises a fluorine-
4 generating species. Preferably the plasma selectivity is for the silicon dioxide over the
5 photoresist material.

6 Figure 1C shows the next step in the process of etching conductive layer 106,
7 where the photoresist layer 112 has been stripped from the surface of pattern masking
8 layer 110. This stripping procedure may be a wet chemical removal or may be a plasma
9 etch which is selective for the photoresist layer 112 over the pattern masking layer 110.
10 Stripping of photoresist layer 112 is carried out for two reasons. The organic-based
11 photoresist materials typically used for layer 112 would melt or become distorted in
12 shape at the temperatures commonly reached during the etching of conductive layer 106.
13 This could lead to distortion of the pattern which is transferred to conductive layer 106.
14 In addition, polymeric species generated due to the exposure of the surface of photoresist
15 layer 112 to the etchant plasma tend to contaminate adjacent surfaces during the etching
16 of conductive layer 106, thereby decreasing the etch rate of conductive layer 106.

17 The procedure of using a photoresist material to pattern an underlying silicon
18 oxide patterning layer is described in U.S. Patent No. 5,067,002 to Zdebel et al., issued
19 November 19, 1991. Zdebel et al. mention the need to remove the photoresist material
20 prior to etching of underlying layers, to avoid contamination of underlying surfaces with
21 the photoresist material during etching of such underlying layers. David Keller describes
22 the use of an ozone plasma for the purpose of dry etch removal of a photoresist mask
23 from the surface of an oxide hard mask in U.S. Patent No. 5,346,586, issued September
24 13, 1994. Mr. Keller also mentions that it is easier to etch selectively to a gate oxide
25 when there is no photoresist present during a polysilicon gate oxide etch step.

26 Figure 1D shows the next step in the etching process, where the desired pattern
27 has been transferred through ARC layer 108, conductive layer 106, and barrier layer 104.
28 Typically all of these layers are metal comprising layers, and a halogen containing

1 plasma can be used to etch the pattern through all three layers. At this point, the problem
2 is the removal of the residual silicon dioxide hard masking material and the removal of
3 residue deposits of the silicon dioxide masking material from adjacent surfaces. The
4 residual hard masking material is present as residual masking layer 110, and the residue
5 deposits as 114 on the surface of the patterned conductive layer 106 and the surface of
6 substrate 102.

7 In the case of the deposit 114 on the surface of patterned conductive layer 106,
8 deposit 114 can trap residual chemical etch reactants under deposit 114 and against the
9 surface of patterned conductive layer 106, leading to subsequent corrosion of conductive
10 layer 106. That corrosion is shown on Figure 1D as 116.

11 In addition, when substrate 102 is a low dielectric constant material, for purposes
12 of reducing electrical interconnect delays, residual masking layer 110 which remains
13 after pattern etching through layers 108, 106, and 104 (as shown in Figure 1D) can
14 deteriorate device performance or cause difficulties in future processing steps
15 (particularly during contact via etch). This makes it important to remove any residual
16 masking layer 110 from the surface of ARC layer 108.

17 Further, when a dielectric layer 118 is applied over the surface of the patterned
18 conductive layer 106, as shown in Figure 1E, if residual masking layer 110 is not
19 removed, a non-planar surface 120 is produced. A non-planar surface creates a number
20 of problems in construction of a multi-conductive-layered device, where additional
21 patterned conductive layers (not shown) are constructed over the surface 120 of dielectric
22 layer 118.

23 With the above considerations in mind, we wanted to develop a patterning
24 system, including a multi-layered structure and a method for its use which would provide
25 for the easy removal of residual masking layer material after completion of the patterning
26 process. During the development of the etching method we discovered a particular etch
27 chemistry which is equally applicable to etching organic dielectric layers for formation of
28 contact structures in conventional metallization processes, and in the formation of

1 damascene and dual damascene structures.

2 3 SUMMARY OF THE INVENTION

4 A first embodiment of the present invention pertains to a method of patterning
5 metal-comprising semiconductor device features and conductive features in general,
6 wherein the method provides for the easy removal of any residual masking layer which
7 remains after completion of a pattern etching process. The method provides for a multi-
8 layered masking structure which includes a layer of high-temperature organic-based
9 masking material overlaid by either a layer of a high-temperature inorganic masking
10 material (such as silicon oxide, silicon nitride, or silicon carbide) which can be patterned
11 to provide an inorganic hard mask, or by a layer of high-temperature imageable organic
12 masking material, such as PPMS, which can be processed and patterned to provide a hard
13 mask. The hard masking material is used to transfer a pattern to the high-temperature
14 organic-based masking material, and then the hard masking material is removed. The
15 high-temperature organic-based (carbon-based) masking material is used to transfer the
16 pattern to an underlying semiconductor device feature. The high-temperature organic-
17 based masking material can be removed from the surface of the patterned semiconductor
18 device feature in a manner which reduces or avoids contamination of the patterned
19 feature surface.

20 In accordance with the present invention, we have developed two patterning
21 systems which enable the patterning of underlying layers at relatively high temperatures,
22 ranging between about 150 °C and about 500 °C, while providing easy removal of any
23 residual masking layer remaining after the patterning process.

24 The first patterning system uses a multi-layered masking structure which includes
25 a layer of high-temperature organic-based masking material overlaid by a layer of a high-
26 temperature inorganic masking material, which is further overlaid by a layer of a
27 patterning photoresist.

28 The patterning method is as follows.

1 a) The layer of photoresist material is imaged and developed into a pattern using
2 techniques known in the art, to produce a patterned mask which can be used to transfer
3 the desired pattern throughout the multi-layered masking structure and eventually
4 through at least one device feature layer as well.

5 b) The patterned photoresist is used to transfer the pattern through

6 i) a layer of high-temperature inorganic masking material; and

7 ii) a layer of high-temperature organic-based masking material.

8 Preferably the pattern transfer through the layer of high-temperature organic-
9 based masking material is via an anisotropic plasma etch technique so that this material
10 is not undercut by the pattern transfer process.

11 c) Residual photoresist which remains after pattern transfer is then removed from
12 the multilayered structure by plasma etch, using the high-temperature inorganic masking
13 layer as an etch stop. The photoresist removal is accomplished using an anisotropic etch
14 process which typically comprises an oxygen-based plasma etch. The anisotropic
15 stripping of the photoresist prevents or at least substantially reduces any etching of the
16 high-temperature organic-based masking material during photoresist removal.

17 d) Optionally, the layer of high temperature inorganic masking material may be
18 removed at this time using a plasma etch technique or a wet etch technique designed to
19 minimize any etching of the organic-based masking material. Preferably, the high
20 temperature inorganic masking material is of a thickness such that it will be
21 automatically removed during etching of a feature layer (step e).

22 (e) The pattern is then transferred from the high-temperature organic-based
23 masking layer through at least one feature layer underlying the high-temperature organic-
24 based masking material.

25 f) Any high-temperature organic-based masking material remaining after feature
26 layer patterning is then easily removed using a plasma etch technique. When the etched
27 feature layer would be corroded or oxidized by an oxygen-based plasma, a
28 hydrogen/nitrogen-based plasma etch technique is recommended. The removal of

1 organic-based masking material may be by a wet stripping technique using a solvent
2 known in the art to be advantageous in the passivation of the surface of the patterned
3 feature layer.

4 Since there is no residual photoresist material remaining from step a) present
5 during etching of the feature layer, there is no layer which is likely to melt or distort in
6 shape during transfer of the pattern from the high-temperature organic-based masking
7 material to an underlying device feature layer.

8 Since the high-temperature organic-based masking layer is easily removed, there
9 need be no residual masking layer present in the device structure to affect device
10 performance or to cause difficulties during subsequent via etch. Preferably, the high-
11 temperature organic-based masking layer is formed from α -C and α -FC films deposited
12 using CVD techniques. Examples of starting materials used to form such films include
13 CH_4 , C_2H_2 , CF_4 , C_2F_6 , C_4F_8 , NF_3 , and combinations thereof; there are, of course, numbers
14 of other carbon-containing precursor materials which can also be used. The starting
15 materials which contain less (or no) fluorine are preferred.

16 The second patterning system is different from the first patterning system in that
17 it uses a high-temperature pattern-imaging layer rather than a more standard photoresist
18 imaging layer. The high-temperature pattern-imaging layer is stable at temperatures
19 ranging from about 150 °C to about 500 °C, compared with photoresist materials which
20 are generally stable at about 150 °C or lower. Preferably the high-temperature pattern-
21 imaging layer is a plasma-polymerized material; more preferably, the pattern-imaging
22 layer is an organo-silicon compound, such as plasma polymerized methyl silane (PPMS),
23 which may be imaged by deep UV and which is plasma-developable. However, the
24 high-temperature imaging layer may also be formed from a different silane-based starting
25 material such as a TEOS-based (tetra-ethyl-ortho-silicate - based) chemistry, and one
26 skilled in the art may select from other similar materials known in the art.

27 The patterning method is as follows.

28 a) A layer of high-temperature imageable material is imaged and developed into

1 a pattern using techniques known in the art, to produce a patterned mask which can be
2 used to transfer the desired pattern through the high-temperature organic-based masking
3 material and eventually through at least one device feature layer.

4 b) After patterning of the high-temperature imageable material, the pattern is
5 transferred through the underlying layer of high-temperature organic-based masking
6 material. Preferably the pattern is transferred via an anisotropic etch technique, whereby
7 the high-temperature organic-based masking material is not undercut by the pattern
8 transfer step.

9 c) The pattern is then transferred from the multi-layered structure formed in steps
10 a) and b) through at least one feature layer underlying the high-temperature organic-
11 based masking material. Preferably the pattern is transferred using an anisotropic etching
12 technique so that any high-temperature imageable material which might remain from step
13 b) is removed during this pattern transfer step. In addition, the use of an anisotropic
14 etching technique reduces or avoids the possibility of undercutting the high-temperature
15 organic-based material layer during the pattern transfer to the underlying device feature
16 layer.

17 d) Any residual high-temperature organic-based masking material which remains
18 after pattern transfer is then easily removed using a plasma etch technique. When the
19 etched feature layer would be corroded or oxidized by an oxygen-based plasma, a
20 hydrogen-based plasma etch technique is recommended.

21 Since there is no low temperature residual photoresist material used during this
22 process, there is no layer which is likely to melt or distort in shape during transfer of the
23 pattern from the high-temperature organic masking material to an underlying device
24 feature layer.

25 As previously mentioned, the high-temperature imageable material is preferably a
26 silane-based starting material such as plasma polymerized methyl silane (PPMS), or a
27 TEOS-based (tetra-ethyl-ortho-silicate - based) material, and one skilled in the art may
28 select from other similar materials known in the art.

1 The high-temperature organic-based masking material is preferably chosen from
2 materials which can be easily removed by plasma etch techniques or by using a solvent
3 known in the art to be advantageous in the passivation of the surface of the patterned
4 feature layer. Examples of such materials are provided above with reference to the first
5 patterning system.

6 When the device feature layer which is to be patterned includes a copper layer,
7 that copper layer is preferably pattern etched using either an enhanced physical
8 bombardment technique or a plasma etching technique which generates sufficient
9 hydrogen to protect the copper surface during patterning.

10 The above-described method is also useful in the pattern etching of aluminum or
11 tungsten, even though these metals can be etched at lower temperatures, typically below
12 about 200 °C (because the etch reaction byproducts are more volatile). When the feature
13 size of an aluminum-comprising structure is about 0.25 μm and smaller, use of a hard
14 mask patterning layer, such as silicon dioxide, silicon nitride, or silicon carbide provides
15 a sufficiently long mask lifetime during etching of an underlying aluminum-comprising
16 layer. Further, since the selectivity toward aluminum is better when such a hard mask
17 patterning layer is used rather than a typical organic-based photoresist, the masking layer
18 thickness can be less, the aspect ratio is lower, and the possibility of shading damage to
19 the device structure is reduced. The present method makes removal of the hard masking
20 material possible without damage to the substrate, which is advantageous in subsequent
21 processing.

22 A second embodiment of the present invention pertains to a specialized etch
23 chemistry useful in the patterning of organic polymeric layers such as low dielectric
24 constant (low k dielectric) materials and other organic polymeric interfacial layers. This
25 etch chemistry is especially useful in a multilayered substrate of the kind described
26 above. It is also useful in etching damascene structures where a metal fill layer is applied
27 over the surface of a patterned organic-based dielectric layer.

28 In particular, when the organic, polymeric material being etched serves as a

1 patterning mask for etch of a copper film, or when the organic, polymeric material being
2 etched is part of a damascene structure which is to be filled with copper, the etch
3 chemistry provides for use of etchant plasma species where the oxygen, fluorine,
4 chlorine, and bromine content is minimized. Preferably, essentially none of the plasma
5 source gas material furnishes reactive species comprising oxygen, fluorine, chlorine, or
6 bromine. When a patterning mask for etch of a copper film is prepared, should these
7 etchant species contact the copper film, the film is oxidized or otherwise corroded. In
8 addition, etchant species which contain oxygen, fluorine, chlorine or bromine leave
9 deposits of etch byproduct on etched contact via and damascene structure surfaces which
10 may cause oxidation and corrosion of copper depositions made over such surfaces.
11 Further, during etching of some organic-comprising materials, oxygen and fluorine
12 etchant species tend to have a detrimental effect on a typical contact via or trench etch
13 profile.

14 When the conductive material is aluminum, tungsten, platinum, or iridium, rather
15 than copper, the presence of oxygen is more acceptable during etch of the organic
16 polymeric material. When the metal fill layer is tungsten, platinum, or iridium, the effect
17 of the presence of fluorine, chlorine and bromine depends on the particular material used,
18 as is known to one skilled in the art. However, even when the conductive material is
19 aluminum, tungsten, platinum or iridium, oxygen-comprising or halogen etchant species
20 are typically used as additives to increase etch rate or improve etch profile, or to control
21 residue on an etch surface, but are not the principal etchant species for etching of the
22 organic, polymeric material.

23 The preferred etch plasma of the present invention is a hydrogen/nitrogen-based
24 plasma, wherein the principal etchant species is hydrogen, or nitrogen, or a combination
25 thereof. In addition, as described above, depending on the materials used in the device
26 fabrication, the concentration of at least one etchant species such as oxygen, chlorine,
27 fluorine, and bromine is preferably minimized. To provide a hydrogen/nitrogen-based
28 plasma, the plasma etchant species comprise principally hydrogen, or principally

1 nitrogen, or principally a mixture thereof. To provide these species, the plasma source
2 gas comprises at least one of the materials selected from the group consisting of
3 hydrogen, nitrogen, ammonia and compounds thereof, hydrazine and compounds thereof,
4 hydroazoic acid, and combinations thereof. When the conductive material to be used in
5 the device is not copper, but is instead aluminum, tungsten, platinum, or iridium, the
6 plasma source gas may comprise hydroxylamine or a compound thereof. The most
7 preferred plasma source gas comprises ammonia; or hydrogen and nitrogen; or a
8 combination of ammonia with hydrogen, nitrogen, or both.

9 Other gases which provide essentially non-reactive etchant species, such as argon,
10 helium, neon, krypton, and xenon may be present in varying amounts, by way of
11 example, and not by way of limitation.

12 In addition, the addition of a small amount of hydrocarbon may be beneficial in
13 the control of etch profile of the high temperature organic polymeric material.

14 It is also possible to use a hydrocarbon-based plasma for etching of the high
15 temperature organic polymeric material. The hydrocarbon-based plasma may optionally
16 include a lesser amount of a component selected from the group consisting of ammonia,
17 hydrogen, nitrogen, and combinations thereof. Other gases which provide essentially
18 non-reactive etchant species, such as argon, helium, neon, krypton, and xenon may also
19 be present in varying amounts, by way of example.

20 When an integrated series of process steps is carried out in a single process
21 chamber and a process step produces a byproduct which includes at least one element
22 harmful to the final device structure, wherein that element is selected from the group
23 consisting of oxygen, fluorine, chlorine, or bromine, it is advisable to dry clean the
24 process chamber subsequent to that process step and prior to proceeding to an etch step
25 using the present method for etching an organic polymeric material. This is particularly
26 important when the feature size of the pattern being etched is 0.25 μm or smaller. As an
27 alternative to repetitive cleaning of process chambers, it is possible to use an integrated
28 processing system which provides several processing chambers which are interconnected

1 in a manner such that a substrate can be passed from chamber to chamber under a
2 controlled environment, and to reserve one of such process chambers for etching using
3 the present method etch chemistry.

4 An economical method of performing the etch techniques described above
5 utilizes a combination of different plasmas wherein the different etchant gases used to
6 create each plasma are sufficiently compatible that all of the etching steps can be carried
7 out in individual (separate) steps in the same etch chamber, if desired. One skilled in the
8 art can select from the various known plasma etchants to obtain the best economies of
9 function which will provide etched features meeting dimensional and surface stability
10 requirements.

11 BRIEF DESCRIPTION OF THE DRAWINGS

12 Figures 1A through 1E show a schematic of the cross-sectional view of a prior art
13 multilayered structure useful in plasma etching (a plasma etch stack), as the etch stack
14 progresses through a series of process steps. This etch stack is generally used for etching
15 of a device feature conductive material layer.

16 Figure 2A shows a schematic of the cross-sectional view of a first preferred
17 embodiment plasma etch stack of the present invention. Figures 2B through 2G show
18 the changes in the etch stack as it progresses through the method steps of the present
19 invention.

20 Figure 3A shows a schematic of the cross-sectional view of a second preferred
21 embodiment plasma etch stack of the present invention. Figures 3B through 3G show
22 the changes in the etch stack as it progresses through the method steps of the present
23 invention.

1 Figure 4A shows a schematic of a cross-sectional view of a series of etched
2 contact vias, where each via is created through a multilayered structure which includes,
3 from top to bottom, a layer of silicon oxide patterned hard mask, and a layer of
4 FLARE™ low dielectric constant material. Underlying the low k dielectric is a layer of
5 titanium nitride, and underlying the titanium nitride is a layer of aluminum. Due to the
6 etch chemistry used to etch the via, the low k dielectric, a poly(arylene ether) is severely
7 undercut beneath the patterning silicon oxide hard mask.

8 Figure 4B shows a schematic of a cross-sectional view of the same etched contact
9 vias shown in Figure 4A, except that the etch chemistry of the present invention was
10 used to provide nearly straight sidewalls on the etched via.

11 Figure 5 is a schematic of a process chamber and auxiliary apparatus of the kind
12 which can be used to carry out the plasma etching steps described herein.

13 Figure 6 is a schematic of a processing system which includes a variety of process
14 chambers which permit transfer of substrates from one chamber to another under a
15 controlled environment. For example, the substrate is not exposed to air or moisture.

16 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

17 In accordance with the present invention, we have developed two patterning
18 systems which enable the patterning of underlying layers while providing for the easy
19 removal of masking layers used to accomplish the patterning. Further, we have
20 developed an etch chemistry which is useful in the pattern etching of organic, polymeric
21 material layers during formation of contact/interconnect structures. The etch may be for
22 mask opening prior to etch of an underlying conductive layer, or may be for preparation
23 of an electrical contact via in a general process, or may be for preparation of a damascene
24 or dual damascene structure.

1 I. DEFINITIONS

2 As a preface to the detailed description, it should be noted that, as used in this
3 specification and the appended claims, the singular forms "a", "an", and "the" include
4 plural referents, unless the context clearly dictates otherwise. Thus, for example, the
5 term "a semiconductor" includes a variety of different materials which are known to have
6 the behavioral characteristics of a semiconductor, reference to "a conductive material"
7 includes aluminum, aluminum alloys, copper, copper alloys, platinum, platinum alloys,
8 iridium, iridium alloys, tungsten, tungsten alloys, combinations thereof, and other
9 conductive materials which would be suitable in the application described.

10 Specific terminology of particular importance to the description of the present
11 invention is defined below.

12 The term " α -C" refers to high temperature amorphous carbon-comprising
13 materials which are typically produced by CVD in a plasma chamber.

14 The term " α -FC" refers to high temperature fluorocarbon materials which are
15 typically produced by CVD in a plasma chamber.

16 The term "aluminum" includes alloys of aluminum of the kind typically used in
17 the semiconductor industry. Such alloys include aluminum-copper alloys, and
18 aluminum-copper-silicon alloys, for example. Typically such alloys of aluminum
19 comprise about 0.5 % copper.

20 The term "anisotropic etching" refers to etching which does not proceed in all
21 directions at the same rate. If etching proceeds exclusively in one direction (e.g. only
22 vertically), the etching process is said to be completely anisotropic.

23 The term "bias power" refers to the power used to control ion bombardment
24 energy and the directionality of ions toward a substrate.

25 The term "copper" refers to copper and alloys thereof, wherein the copper content
26 of the alloy is at least 80 atomic % copper. The alloy may comprise more than two
27 elemental components.

28 The term "feature" refers to metal lines and openings on a substrate, and other

1 structures used to form a semiconductor device.

2 The term "high density plasma" refers to, but is not limited to, a plasma having an
3 electron density of at least $5 \times 10^{10} \text{ e}^-/\text{cm}^3$.

4 The term "hydrogen-based plasma" refers to a plasma having a sufficiently high
5 hydrogen content to reduce the corrosion of the exterior surfaces of etched features by
6 incident reactive species which are present due to etching of adjacent surfaces. A
7 preferred example of a hydrogen-based plasma is described in co-pending application
8 Serial No. 08/911,878, filed August 13, 1997.

9 The term "hydrogen/nitrogen-based plasma" refers to a plasma having principally
10 hydrogen-comprising and/or nitrogen-comprising etchant species. In addition,
11 depending on the materials used in the device fabrication, the concentration of at least
12 one etchant species generated from a source comprising an element selected from the
13 group consisting of oxygen, chlorine, fluorine, and bromine is minimized. A preferred
14 plasma source gas for producing a hydrogen/nitrogen-based plasma comprises ammonia;
15 or hydrogen and nitrogen; or a combination of ammonia with hydrogen, nitrogen, or
16 both. Other essentially chemically inert components such as argon, helium, neon,
17 krypton, and xenon may be present in varying amounts, by way of example, and not by
18 way of limitation.

19 The term "hydrocarbon-based plasma" refers to a plasma having principally
20 hydrogen and carbon-comprising etchant species. The hydrocarbon-based plasma may
21 optionally include a lesser amount of a component selected from the group consisting of
22 ammonia, hydrogen, nitrogen, and combinations thereof. Other gases which provide
23 essentially non-reactive etchant species may be present in varying amounts. In addition,
24 depending on the conductive material to be used in the device structure, the plasma
25 source gas may contain an additive element or compound (for purposes of controlling
26 etch rate or profile) which generates up to about 30 atomic % or less of the total etchant
27 species, where such additive etchant species comprises oxygen, or fluorine, or chlorine,
28 or bromine. Preferred plasma source gases for producing a hydrocarbon-based plasma

1 comprises methane or α -carbon.

2 The term "ion bombardment" refers to physical bombardment by ions (and other
3 excited species of atoms which are present with the ions) to remove atoms from a
4 surface, where physical momentum transfer is used to achieve the atom removal.

5 The term "isotropic etching" refers to an etching process where etching can
6 proceed in all directions at the same rate.

7 The term "oxygen-based plasma" refers to a plasma which is rich in oxygen
8 content either in neutral or charged form. The plasma may include additives comprising
9 nitrogen, or hydrogen, or chlorine, or fluorine, or carbon, by way of example and not by
10 way of limitation. Additives such as CF_4 , CH_4 and NH_3 are commonly used.

11 The term "plasma" refers to a partially ionized gas containing an equal number of
12 positive and negative charges, as well as some other number of non-ionized gas particles.

13 The term "plasma-polymerized methysilane" refers to a new deep UV resist
14 material which is deposited from a low power RF plasma discharge in methysilane at
15 room temperature. This material possesses an amorphous organosilicon hydride network
16 structure. While initially opaque in the deep UV (i.e. 248 nm), a typical 0.25 micron
17 thick film undergoes efficient photooxidation with bleaching to form glass-like siloxane
18 network material.

19 The term "shading damage" refers to, but is not limited to, damage to device
20 structures which occurs when a conductive feature becomes charged with ions, as
21 electrons are trapped by the mask over a high aspect ratio feature, creating a voltage
22 across device features which results in a shift in the performance parameters of the
23 device.

24 The term "source power" refers to the power used to generate ions and neutrals
25 whether directly in an etching chamber or remotely as in the case of a microwave plasma
26 generator.

27 The term "substrate" includes semiconductor materials, glass, ceramics,
28 polymeric materials, and other materials of use in the semiconductor industry.

II. AN APPARATUS FOR PRACTICING THE INVENTION--

The preferred embodiment etch processes described herein were carried out in a CENTURA® Integrated Processing System available from Applied Materials, Inc. of Santa Clara, California. The system is shown and described in United States Patent No. 5,186,718, the disclosure of which is hereby incorporated by reference. This equipment included a Decoupled Plasma Source (DPS) of the kind described by Yan Ye et al. at the Proceedings of the Eleventh International Symposium of Plasma Processing, May 7, 1996 and as published in the Electrochemical Society Proceedings, Volume 96-12, pp. 222 - 233 (1996). The plasma processing chamber enables the processing of an 8 inch (200 mm) diameter silicon wafer.

A schematic of the processing chamber is shown in Figure 5 which shows an etching process chamber 510, which is constructed to include at least one inductive coil antenna segment 512 positioned exterior to a dielectric, dome-shaped ceiling 520, and connected to a radio frequency (RF) power generator 518. Interior to the process chamber is a substrate 514 support pedestal 516 which is connected to an RF frequency power generator 522 through an impedance matching network 524, and a conductive chamber wall 530 which serves as the electrical ground 534.

The semiconductor substrate 514 is placed on the support pedestal 516 and gaseous components are fed into the process chamber through entry ports 526. A plasma is ignited in process chamber 510 using techniques well known in the industry. Pressure interior to the etch process chamber 510 is controlled using a vacuum pump (not shown) and a throttle valve 527 connected to a process chamber gas exit line 528. The temperature on the surface of the etch chamber walls is controlled using liquid-containing conduits (not shown) which are located in the walls of the etch chamber 510. For experimental purposes, it was desired to maintain the substrate temperature above about 150 °C and below about 350 °C, and this was accomplished using a resistivity heater applied to the substrate support pedestal. The surface of the etching chamber 510

1 walls was maintained at about 80 °C using the cooling conduits previously described. In
2 the case of a production process, preferably, the substrate support platen provides for
3 backside heating or cooling of the substrate.

4 Figure 6 is a schematic of a processing system 600 which includes a variety of
5 process chambers which permit transfer of substrates from one chamber to another under
6 a controlled environment. Typically, a processing system 600 includes etch chambers
7 602 and 604 (which are preferably etch chambers where the power source for plasma
8 generation is separately controlled from the power source used to apply bias to a
9 substrate). In addition, system 600 frequently includes stripping-passivation chambers
10 606 and 608 which provide for the removal of contaminants from the etched surface; a
11 substrate orienter 612; a cool-down chamber 610, and loadlocks 614 and 616.

12 III. A FIRST PREFERRED EMBODIMENT ETCH STACK 13 AND ITS METHOD OF USE

14 Figures 2A - 2G illustrate the first preferred embodiment etch stack of the present
15 invention as it progresses through method steps used in preparing a device structure.
16 Figures 2A through 2C show the opening of a masking structure in preparation for etch
17 of an underlying conductive layer; Figures 2D through 2F show etching of the
18 conductive layers; and Figure G shows the application of a "capping" dielectric layer.
19 Figure 2 A shows the complete etch stack, including: Substrate 212, which was a
20 dielectric layer of silicon dioxide approximately 1,000 Å thick overlying a silicon wafer
21 surface (not shown). A layer 214, of tantalum nitride approximately 500 Å thick was
22 deposited over substrate 212. A layer 216 of copper approximately 8,000 Å thick was
23 deposited over barrier layer 214. A layer 218 of tantalum nitride about 500 Å thick,
24 which served as a barrier layer, was deposited over copper layer 216. A layer 220 of a
25 high-temperature organic-based pattern masking material comprising α -FC was
26 deposited over tantalum nitride layer 218 using a high density plasma CVD technique, to
27 produce a layer approximately 8,000 Å thick. A silicon dioxide pattern masking layer

1 222, approximately 1,000 Å thick, which served as a high-temperature inorganic masking
2 material, was applied over the high-temperature α -FC layer 220. And, finally, a
3 photoresist imaging layer 224, of I - line stepper material (any of these materials which
4 are commonly used in the art are acceptable) approximately 10,000 Å thick was applied
5 over the surface of high-temperature inorganic masking material layer 222.

6 In Figure 2A, I - line photoresist imaging layer 224 has already been patterned to
7 provide the feature shape desired to be transferred to the silicon dioxide pattern masking
8 layer 222 and high-temperature organic-based masking layer 220. Preferably, the
9 thickness of photoresist imaging layer 224 is designed so that it is nearly totally
10 consumed during transfer of the pattern through the high-temperature inorganic masking
11 layer 222 and high-temperature organic-based masking layer 224.

12 Figure 2B shows the plasma etching stack described in Figure 2A, where the
13 pattern in photoresist imaging layer 224 has been transferred through the high
14 temperature silicon dioxide inorganic pattern masking layer 222 and slightly into the α -
15 FC-comprising layer 220. This pattern transfer was accomplished in the Centura®
16 Integrated Processing System previously described, using a fluorine-containing plasma
17 of the kind generally known in the art for etching silicon dioxide. During the etching of
18 silicon dioxide layer 222, the plasma feed gas to the process chamber was about 100
19 sccm of argon and 30 sccm of CHF_3 . The substrate temperature during etching was
20 about 20 °C, with the process chamber walls at about 80 °C. The process chamber
21 pressure during etching was about 10 mT. The source power to the plasma inducing coil
22 was about 1800 W @ 2 MHZ and the bias power to the substrate support platen was
23 about 300 W @ 13.56 MHZ. A plasma was ignited using techniques standard in the art,
24 and the time period required for pattern transfer through silicon dioxide layer 222 was
25 approximately 15 seconds. Subsequently, without extinguishing the plasma, the plasma
26 feed gas was changed to an oxygen-based plasma for etching the α -FC layer 220. The
27 plasma feed gas to the process chamber was 100 sccm of O_2 , and 10 sccm of N_2 . The
28 substrate temperature during etching was about 20 °C, with the process chamber walls at

1 about 80 °C. The process chamber pressure during etching was about 10 mT. The
2 source power to the plasma inducing coil was about 1000 W @ 2 MHZ and the bias
3 power to the substrate support platen was about 250 W @ 13.56 MHZ. The time period
4 required for pattern transfer through α -FC layer 220 was approximately 80 seconds. An
5 alternative to using this oxygen-based plasma is to use the hydrogen/nitrogen-based
6 plasma etch chemistry of the present invention, which will be discussed in detail
7 subsequently.

8 Figure 2C shows the plasma etching stack described in Figure 2B, after removal
9 of residual photoresist imaging layer 224. Residual photoresist imaging layer 224 was
10 removed using the oxygen-based plasma and etch conditions described with reference to
11 the α -FC layer 220, with an etch time period of about 20 seconds. The
12 hydrogen/nitrogen-based plasma etch chemistry could be used for removal of this
13 photoresist layer as well. The underlying layer 222 of silicon dioxide was used as an
14 etch stop over high-temperature organic-based layer 220, while tantalum nitride barrier
15 layer 218 was used as the etch stop protecting copper layer 216 from oxidation. The
16 plasma and process conditions described above provided anisotropic stripping of
17 photoresist imaging layer 224, so that high-temperature α -FC masking layer 220 would
18 not be undercut during the removal of residual photoresist imaging layer 224.

19 It is preferable to use the hydrogen/nitrogen-based etch chemistry for etching
20 both photoresist layer 224 and high-temperature organic-based layer 220 when copper is
21 the conductive layer, as this reduces the potential for oxidation of the copper.

22 Figure 2D shows an optional step in which the layer 222 of silicon dioxide may
23 be removed. However, for most applications, such as this application where feature layer
24 216 comprises a metal (copper), if the thickness of silicon dioxide layer 222 is properly
25 designed, this layer will be automatically removed during the patterning of feature layer
26 216. Preferably the etch selectivity of the materials is such that layer 222 etches more
27 rapidly than layer 220, so that the desired mask profile is obtained.

28 Figure 2E shows the plasma etching stack after transfer of the pattern through

1 tantalum nitride barrier layer 218, copper layer 216, and tantalum nitride barrier layer
2 214 to the upper surface of silicon dioxide dielectric layer 212. This etching of the
3 conductive copper layer 216 and accompanying barrier layers 218 and 214 was
4 accomplished using a feed gas to the process chamber of 70 sccm of HCl, 50 sccm of
5 N₂, and 5 sccm of BCl₃. The substrate temperature during etching was about 250 °C,
6 with the process chamber walls at about 80 °C. The process chamber pressure during
7 etching was about 20 mT. The source power to the plasma inducing coil was about
8 1,500 W @ 2 MHZ and the bias power to the substrate support platen was about 600 W
9 @ 13.56 MHZ. The end point of etch through tantalum nitride barrier layer 214 was
10 measured by optical monitoring using a sensor measuring at a wavelength of about 3,590
11 Å. The time period required for pattern transfer through the tantalum nitride barrier
12 layer 218, copper layer 216, and tantalum nitride barrier layer 214 was about 150
13 seconds. A hydrogen-based etch chemistry was used during patterning of the copper
14 feature layer 216 to avoid corrosion of the copper. This hydrogen-based etch chemistry
15 uses HCl as its principal etchant species source (to produce hydrogen and chlorine-
16 comprising etchant species), and is distinguishable from a hydrogen/nitrogen-based etch
17 chemistry which uses principally hydrogen-comprising and/or nitrogen-comprising
18 etchant species.

19 Depending on the relative thicknesses of layers α -FC layer 220, tantalum nitride
20 218, copper layer 216, and tantalum nitride layer 214, and the etching conditions used,
21 there should be enough of the α -FC layer 220 remaining at the end of the etch process to
22 provide CD (critical dimension) control. Therefore, a separate process is needed to
23 remove the remaining portion of this α -FC layer. The process for stripping the α -FC
24 layer may be carried out in the feature patterning etch chamber or in a downstream
25 plasma chamber.

26 Figure 2F shows the patterned copper feature layer 216 with accompanying
27 barrier layers 214 and 218, after removal of the remaining portion of the α -FC layer 220.
28 The α -FC layer 220 may be removed via anisotropic stripping using a hydrogen-based

chemistry of the kind described above. The α -FC layer may also be removed using a wet stripping process using a solvent which assists in the passivation of the etched copper feature surface. In the present instance, a hydrogen/nitrogen-based plasma was used in combination with an anisotropic dry stripping technique, wherein the feed gas to the process chamber was 100 sccm of H_2 . The substrate temperature during etching was about 45 °C, with the process chamber walls at about 80 °C. The process chamber pressure during etching was about 10 mT. The source power to the plasma-inducing coil was about 1,000 W @ 2 MHz and the bias power to the substrate support platen was about 200 W @ 13.56 MHz. The time period required for stripping of the remaining portion of the α -FC layer 220 was about 120 seconds. If the conductive layer 216 had been aluminum, tungsten, platinum, or iridium, an oxygen-based plasma could have been used to remove the α FC layer 220 without concern about corrosion of the conductive layer.

Figure 2G shows the application of a dielectric capping layer 230 of a low dielectric constant material such as an α -C or an α -FC over patterned tantalum nitride layer 218, copper layer 216, tantalum nitride layer 214, and silicon dioxide substrate 212. The capping layer 230 provided electrical isolation between the conductive copper layer 216 and the surrounding environment. Due to the thinness of tantalum nitride layer 218, the upper surface 219 of the structure was far more planar than the surface 120 observed for the prior art planarization layer illustrated in Figure 1E. Preferably the α -C or an α -FC is applied using a vapor deposition technique known in the art, although spin-on techniques, for example, are also acceptable.

One skilled in the art will recognize that high-temperature inorganic masking materials other than silicon oxide can be used as the capping layer overlying the high-temperature organic-comprising masking material. In addition, one skilled in the art will recognize that high-temperature organic-based masking materials other than α -FC, such as α -C, polyimide, parylene, and teflon, for example, can be used. Anti-reflective/barrier layer materials other than tantalum nitride, such as silicon oxynitride, tantalum, titanium

1 nitride, tungsten titanate, and tungsten nitride may also be used. And finally, the method
2 is not limited to the etching of device features which utilize copper as the conductive
3 material. Other conductive materials which require high etch temperatures (in excess of
4 about 200 °C), such as platinum, silver, gold, iridium, for example, can be used. Further
5 the method offers advantages in the etching of conductive materials which require lower
6 etch temperatures (below about 200 °C), such as aluminum or tungsten, when the
7 feature size is below about 0.25 μm and selectivity to the conductive material over
8 masking materials makes control of the etch process difficult.

9 Figures 2A through 2C can also be used to describe a second embodiment of the
10 present invention in which the specialized etch chemistry previously described is used to
11 prepare a contact via structure. If the conductive material shown in Figures 2A through
12 2C did not form a layer 216 (as shown) but instead formed a series of lines which ran
13 perpendicular into the page and parallel to each other at locations 221 (surrounded by an
14 inter-metal dielectric), openings 223 could be used to form contact vias by deposition of
15 a conductive fill material (not shown) therein. By way of explanation, with reference to
16 Figures 2A through 2C, if layer 220 is a low k dielectric (or other dielectric organic
17 polymer layer), subsequent to patterning of the layer, a diffusion barrier layer and/or a
18 wetting layer (not shown) is applied over the etched surfaces, followed by deposition of a
19 conductive layer (not shown). The excessive conductive material (not shown) overlying
20 the mask patterning layer 222 (and mask patterning layer 222, if desired) is then removed
21 either by etch back or by chemical-mechanical polishing.

22 IV. A SECOND PREFERRED EMBODIMENT ETCH STACK 23 AND ITS METHOD OF USE

24 Figures 3A - 3G illustrate the second preferred embodiment etch stack of the
25 present invention and its progression through the method steps of the present invention.
26 Figure 3 A shows the complete etch stack, including: Substrate 312, which was a
27 dielectric layer of silicon dioxide approximately 10,000 Å thick overlying a silicon wafer

1 surface (not shown). A barrier layer 314, of tantalum nitride approximately 500 Å thick
2 was deposited over substrate 312. A layer 316 of copper approximately 8,000 Å thick
3 was deposited over barrier layer 314. A layer 218 of tantalum nitride about 500 Å thick
4 was deposited over copper layer 216. A layer 220 of a high-temperature organic-based
5 pattern masking material comprising α -FC was deposited over titanium nitride layer 218
6 using a high density plasma CVD technique, to produce a layer approximately 8,000 Å
7 thick. And, finally, a layer 322 of plasma polymerized methylsilane (PPMS) was
8 deposited from a low power RF plasma discharge in methylsilane at room temperature,
9 to produce a layer approximately 1,000 Å thick.

10 Subsequently, the PPMS layer was imaged using deep UV in the presence of
11 oxygen to produce a glass-like siloxane pattern 324 within PPMS layer 322, as shown in
12 Figure 3B. Figure 3C illustrates the pattern development of the PPMS high
13 temperature imaging layer 324, which was developed using chlorine plasma etching by
14 techniques known in the art (as described by T.W. Weidman et al., Journal of
15 Photopolymer Science and Technology, Volume 8, Number 4, 679 - 686 (1995)).

16 Subsequently, as shown in Figure 3D, the underlying α -FC layer 320 was etched
17 using an oxygen-based plasma in the manner described above with reference to Figure
18 2B, where α -FC layer 220 was patterned. The time period required for pattern transfer
19 through α -FC layer 320 was approximately 80 seconds. The oxygen-based plasma
20 chemistry was chosen so that the patterned silicon dioxide 324 formed from the high-
21 temperature imageable material (PPMS) layer 322 and tantalum nitride barrier layer 318
22 would not be attacked during etching of α -FC layer 320. The oxygen-based etch
23 conditions referenced above provided anisotropic etch conditions so that undercutting of
24 the α -FC layer 320 during pattern development was avoided.

25 Figure 3E shows the transfer of the pattern through tantalum nitride barrier layer
26 318, copper layer 316, and tantalum nitride barrier layer 314 to the upper surface of
27 silicon dioxide dielectric layer 312. This etching of the conductive copper layer 316 and
28 accompanying barrier layers 318 and 314 was accomplished using the method described

1 with reference to Figure 2E.

2 Depending on the relative thicknesses of layers α -FC layer 320, tantalum nitride
3 318, copper layer 316, and tantalum nitride layer 314 and the etching conditions used,
4 there should be enough of the α -FC layer 320 remaining at the end of the etch process to
5 provide CD (critical dimension) control. Therefore, a separate process is needed to
6 remove the remaining portion of this α -FC layer. The process for stripping the α -FC
7 layer may be carried out in the feature patterning etch chamber or in a downstream
8 plasma chamber.

9 Figure 3F shows the patterned feature layer 316 with accompanying barrier layers
10 318 and 314, after removal of the remaining portion of the α -FC layer 320. Preferably the
11 α -FC layer 320 is removed via anisotropic stripping using a hydrogen based chemistry of
12 the kind described above or a wet stripping process using a solvent which assists in the
13 passivation of the etched copper feature surface. In the present instance, an anisotropic
14 dry stripping technique, as described with reference to Figure 2F was used.

15 Figure 3G shows the application of a planarization layer 328 of a low dielectric
16 constant material such as an α -C or an α -FC over the patterned tantalum nitride layer
17 318, copper layer 316, tantalum nitride layer 314, and silicon dioxide substrate 312. The
18 inter-metal dielectric layer exhibited a relatively planar surface, compared with the non-
19 planar surface 120 observed for the prior art planarization layer illustrated in Figure 1E.
20 Preferably the α -C or an α -FC is applied using a vapor deposition technique known in the
21 art, although spin-on techniques, for example, are also acceptable.

22 One skilled in the art will recognize that other precursor materials can be used to
23 create a photosensitive siloxane material similar to PMMS, to produce a satisfactory
24 mask layer for pattern transfer to the high-temperature organic-comprising masking
25 material. In addition, one skilled in the art will recognize that other high-temperature
26 organic-based masking materials, ARC materials, barrier layer materials, and conductive
27 materials, such as those previously listed (and not by way of limitation) can be used.

28 It is important to mention that when copper is used as the conductive material, the

1 etching methods disclosed in U.S. Application Serial No. 08/891,410, and 08/911,878,
2 referenced above, are recommended for use in combination with the methods of the
3 invention described herein.

4 In particular, Application Serial No. 08/891,410 discloses that copper can be
5 pattern etched at acceptable rates and with selectivity over adjacent materials using an
6 etch process which utilizes a solely physical basis such as ion bombardment, without the
7 need for a chemically based etch component.

8 A first preferred enhanced physical bombardment technique requires an increase
9 in ion density and/or an increase in ion energy of ionized species which strike the
10 substrate surface. An increase in ion density is preferably achieved by placing a device
11 inside the etch chamber above the substrate surface, which device enables an increase in
12 the number of ionized particles striking the substrate surface. An example of such a
13 device is an inductive coil which is used to create a high density plasma having an
14 increased number of active species or to maintain the number of active species supplied
15 by another source so that an increased number of ionized species are available to strike
16 the substrate surface.

17 A second preferred method for increasing the number of ionized species is to feed
18 into the process chamber a microwave-generated plasma produced outside of the
19 chamber. It is also possible to increase the number of ionized species by increasing the
20 RF power to an external inductively coupled coil or to increase the DC power to a
21 capacitively coupled source for ion species generation. However, these latter two
22 techniques are less preferred methods for increasing ion density, since the copper (and
23 alloy metal(s)) atoms generated during etching affect the performance of an external coil
24 and since capacitively coupled species generation is not very efficient. By ion energy, it
25 is meant the energy of the ion at the time it strikes the substrate surface. A second
26 preferred enhanced physical bombardment technique is increasing (to the limit that the
27 substrate is detrimentally affected) the ion energy. Ion energy may be increased by
28 increasing an offset bias on the substrate which attracts the ionized species toward the

1 substrate. This is typically done by increasing the RF power to a platen on which the
2 substrate sets. The effectiveness of an increase in the bias power is dependent upon the
3 RF frequency and the ratio of the bias grounding area to the surface area of the substrate.
4 Ion energy is further increased by operating the etch process chamber at a lower pressure,
5 typically down to about 20 mT, depending on the gases present.

6 A technique which is beneficial in tuning the physical bombardment used in a
7 sputtering process is a pulsing of the ion density or the ion energy. One preferred means
8 of pulsing the ion energy is to pulse the power to the device which produces the ion
9 species or which is used to increase or maintain the number of ionized species available
10 to strike the substrate surface. Such pulsing is preferably applied to a device located
11 internally within the process chamber. The pulsing may be of the feed rate of an
12 externally-generated plasma into the process chamber. Less preferably, the pulsing may
13 be applied to an external inductively coupled source for plasma generation or to a
14 capacitively coupled source for plasma generation. An even more preferred means of
15 pulsing the ion energy is by pulsing the power to the offset bias source which is applied
16 to the substrate. Pulsing of the ion energy reduces the possibility that an excited copper
17 atom leaving the copper surface during etching will reattach to the copper surface in an
18 adjacent location. The pressure in the process vessel may also be pulsed as a means of
19 pulsing the ion energy.

20 Another technique which is beneficial in tuning the physical bombardment is the
21 use of thermal phoresis. Thermal phoresis occurs when the temperature of the substrate
22 surface is higher than the temperature of the etch chamber surfaces (walls), whereby
23 particles dislodged from the higher temperature substrate surface are attracted toward the
24 colder chamber surfaces, whereby improved removal of copper from the etch surface is
25 achieved.

26 It is possible to use a combination of physical ion bombardment with a
27 chemically reactive ion component, so long as the concentration of the chemically
28 reactive ion component is sufficiently low that the etching is carried out in a physical

1 bombardment dominated etch regime. Preferably this combination technique is carried
2 out at temperatures above about 150 °C and at pressures below about 50 mT. Since the
3 additional energy provided by the physical bombardment is added to the formation of
4 volatile chemical reaction-generated compounds, the copper removal rate is not limited
5 solely to the rate of formation of the volatile compounds and the ability of a low process
6 chamber pressure to facilitate removal of such volatile compounds. When physical ion
7 bombardment dominates the etch process, the pressure in the process chamber can be
8 adjusted, to permit increased ion bombardment. An overall synergistic effect occurs,
9 enhancing the copper atom removal rate. The preferred chemically reactive ion species
10 is a halogen-comprising species or compound having a low molecular weight, such as
11 Cl₂, HCl, BCl₃, HBr, CHF₃, CF₄, SiCl₄, and combinations thereof. When a chlorine-
12 comprising species is used, the chlorine-comprising components present in the feed gases
13 to the etch chamber should be no greater than 30 volume % of the gases fed into the etch
14 chamber during the patterned copper etch. A passivating agent such as N₂, NH₃, and
15 CH₄ may be used in combination with the chemically reactive ion species. The content
16 of copending application Serial No. 08/ 891,410 is hereby incorporated by reference in
17 its entirety.

18 Application Serial No. 08/ 911,878 describes an alternative copper etching
19 technology which employs HCl and HBr chemistries in a manner which protects copper
20 from corrosion during the etching process. In particular, copper can be pattern etched in
21 the presence of HCl or HBr while providing the desired feature dimension and integrity if
22 the surface of the copper feature being etched is properly protected during etching. To
23 avoid the trapping of reactive species which can act as a corrosive agent interior of the
24 etched copper surface, hydrogen is applied to that surface. Hydrogen is adsorbed on the
25 copper exterior surface and may be absorbed through the exterior surface of the copper
26 into the bulk copper, so that it is available to react with species which would otherwise
27 penetrate that exterior surface and react with the copper interior to that surface.
28 Sufficient hydrogen must be applied to the exterior surface of the etched portion of the

1 copper feature to prevent incident reactive species present due to etching of adjacent
2 feature surfaces from penetrating the previously etched feature exterior surface.

3 Although any plasma feed gas component comprising hydrogen, which is capable
4 of generating sufficient amounts of hydrogen, may be used, the most preferred
5 embodiment of the invention provides for the use of a component which contains both
6 hydrogen and halogen. Preferred examples are hydrogen chloride (HCl) and/or hydrogen
7 bromide (HBr), which are used as the principal source of the reactive species for etching
8 copper. Dissociation of the HCl and/or HBr provides large amounts of hydrogen for
9 protection of etched copper surfaces, thereby preventing penetration by reactive species
10 adjacent the etched surface. Additional hydrogen gas may be added to the plasma feed
11 gas which comprises the HCl and/or HBr when the reactive species density in the etch
12 process chamber is particularly high. The hydrogen-releasing, halogen-comprising
13 plasma feed gas component may be used as an additive (producing less than 40 % of the
14 plasma-generated reactive species) in combination with other plasma etching species.

15 When HCl and/or HBr is used as the principal source of reactive species for the
16 copper etching, the HCl or HBr are the source for at least 40 %, and more preferably at
17 least 50 %, of the reactive species generated by the plasma. Other reactive species may
18 be used for purposes of feature surface passivation during etching or for purposes of
19 feature surface protection after completion or near the completion of feature surface
20 etching. The species added for surface passivation or surface protection during etching
21 of the copper feature preferably make up 30 % or less, or more preferably make up 10 %
22 or less of the plasma-generated reactive species. By way of example, additional gases
23 which may be added to the plasma feed gas include CH₄, CH₃F, BCl₃, N₂, NH₃, SiCl₄,
24 CCl₄, and CHF₃. Plasma feed gases may include additional inert (non-reactive with
25 copper) gases such as argon, helium, or xenon, to enhance the ionization, or dissociation,
26 or to dilute the reactive species. The critical feature is the availability of hydrogen at the
27 feature surface during the etching process. The content of U.S. Application Serial No.
28 08/911,878 is hereby incorporated by reference in its entirety.

1 Figures 3A through 3D can also be used to describe a second embodiment of the
2 present invention in which the specialized etch chemistry previously described is used to
3 prepare a contact via, in the manner described with reference to Figures 2A through 2C.
4 In this instance the location of the conductive lines is indicated by identification number
5 321, with openings 323 showing the contact vias into which a conductive material is
6 deposited. By way of explanation, with reference to Figures 3A through 3D, if layer 320
7 is a low k dielectric (or other dielectric organic polymer layer), subsequent to patterning
8 of the layer, a diffusion barrier layer and/or a wetting layer (not shown) is applied over
9 the etched surfaces, followed by deposition of a conductive layer (not shown). The
10 excessive conductive material (not shown)overlying the mask patterning layer 324 (and
11 mask patterning layer 324, if desired) is then removed either by etch back or by
12 chemical-mechanical polishing.

13 14 V. APPLICATION OF THE METHOD OF THE INVENTION 15 FOR ETCHING ALUMINUM

16 During discussion of the preferred embodiments of the invention above, it was
17 mentioned that the invention is also useful for conductive materials which can be etched
18 at lower temperatures (below about 200 °C), and particularly for aluminum and tungsten.
19 Although standard photoresist materials can be used as the masking material for
20 aluminum when feature size of the pattern is larger than about 0.25 μm , at smaller feature
21 sizes selectivity becomes a problem. At these smaller geometries, as etching progresses,
22 the structural angles involved results in more rapid deformation of the masking pattern
23 profile, affecting the etch profile. With this in mind, it is necessary to transfer the pattern
24 from the photoresist into a thicker and/or more stable masking material which can
25 maintain the desired pattern profile for a longer time period in the aluminum etch plasma.
26 A thicker masking material results in an increased aspect ratio which can lead to shading
27 damage of underlying device structures, as previously described. With this in mind, a

1 more stable hard masking material such as silicon oxide or silicon nitride is preferable.
2 This masking material, which provides better etch selectivity toward aluminum, can be a
3 thinner patterned layer and still provide the etch time necessary to transfer the desired
4 pattern to underlying layers.

5 However, when a hard masking material is used, the problem of removal of the
6 residual masking material occurs, as previously described. Often the hard masking
7 material is a silicon oxide and the substrate underlying a patterned aluminum
8 interconnect structure is also silicon oxide. This makes it difficult to remove the masking
9 material without damaging the substrate.

10 It is possible to leave residual hard masking material atop a patterned aluminum
11 feature, but this affects the functionality of the finished device. To improve the
12 operational speed of the device, it is preferable to use a low k dielectric as the inter-metal
13 dielectric (for filling gaps between lines and as the dielectric layer which is etched to
14 provide for contact vias). The effectiveness of the low k dielectric in increasing device
15 speed is substantially impacted by the presence of residual high dielectric constant
16 material such as silicon dioxide. Further, if a residue of silicon dioxide remains on top of
17 a metal structure which is to become part of a multi-layer metal device, there may be a
18 problem in subsequent process steps. When a silicon dioxide hard mask is used for
19 pattern transfer through an organic polymeric dielectric overlying the metal structure,
20 prior to reaching the metal surface the etching may stop on silicon dioxide residue
21 overlying the surface of the metal structure.

22 The method of the present invention makes it possible to use easily removable
23 masks which are more resistant to aluminum etch plasmas than photoresist.

24 When aluminum is the metal layer being patterned, the method is the same as
25 described with reference to the First and Second Preferred Embodiments, as described
26 with respect to Figures 2A through 2G and Figures 3A through 3G, with the following
27 major exceptions (there may be other minor differences which will be understood and
28 appreciated by one skilled in the art). Typically the barrier layer is titanium nitride

1 rather than tantalum nitride; the substrate temperature during etching of the aluminum
2 layer is less than about 150 °C, preferably less than about 90 °C, with the process
3 chamber walls at about 80 °C. Plasma source gas composition during etching of the
4 aluminum layer will typically be 150 - 30 sccm of Cl₂/ 100 - 0 sccm of BCl₃/ 0 - 40
5 sccm N₂/ 0 - 20 sccm CH_xF_y (where x ranges from 0 to about 4 and y ranges from 0 to
6 about 4). The process chamber pressure during etching generally ranges between about
7 5 mT and 50 mT. The source power to the plasma-inducing coil typically ranges from
8 about 500 W to about 2,000 W @ 2 MHZ and the bias power to the substrate support
9 platen ranges from about 50 to about 250 W @ 13.56 MHZ.

10 When the high temperature organic-based masking material used in the present
11 invention is a low k dielectric material, for example but not by way of limitation,
12 Poly(arylene)ethers, Poly(arylene)ether oxazoles, Parylene-N, Polyimides,
13 Polynaphthalene-N, Polyphenyl-Quinoxalines, Polybenzoxazoles, Polyindane,
14 Polynorborene, Polystyrene, Polyphenyleneoxide, Polyethylene, Polypropylene,
15 divinylsiloxane bis-benzocyclobutene (BCB), or αC, this may offer an added advantage
16 when a low k dielectric material is also be used to form the electrically insulating layer
17 which is applied over the patterned metal layer.

18 19 VI. SPECIALIZED ETCH CHEMISTRY USEFUL 20 IN COMBINATION WITH THE ETCH STACK

21 A second embodiment of the present invention pertains to a specialized etch
22 chemistry useful in patterning silicon-free organic polymeric layers such as low k
23 dielectrics and other organic interfacial layers. This etch chemistry is particularly useful
24 when the conductive material in a multilayered etch stack is copper, or when copper is
25 the conductive fill material used for formation of a contact via, or in a damascene or dual
26 damascene process.

27 By way of explanation, in a damascene process, the process steps would typically
28 include: blanket deposition of a dielectric material; patterning of the dielectric material

1 to form openings; deposition of a diffusion barrier layer and, optionally, a wetting layer
2 to line the openings; deposition of a conductive layer such as copper, tungsten, or
3 aluminum onto the substrate in sufficient thickness to fill the openings; and removal of
4 excessive conductive material from the substrate surface using chemical-mechanical
5 polishing (CMP) techniques or etch-back techniques. The damascene process is
6 described in detail by C. Steinbruchel in "Patterning of copper for multilevel
7 metallization: reactive ion etching and chemical-mechanical polishing", *Applied Surface*
8 *Science* 91 (1995) 139 - 146.

9 In particular, the etch chemistry of the present invention provides for use of
10 etchant plasma species wherein the content of at least one etchant species selected from
11 the group consisting of oxygen, fluorine, chlorine, and bromine is minimized.
12 Preferably, when the conductive material is copper, essentially none of the plasma source
13 gas material furnishes reactive species comprising oxygen, fluorine, chlorine, or bromine.
14 Etchant species which contain oxygen, fluorine, chlorine or bromine leave deposits of
15 etch byproduct which are chemically harmful to the copper structures which they
16 contact, typically reducing the conductivity of such layers. Further, oxygen etchant
17 species tend to have a detrimental effect on a typical contact via or trench wall etch
18 profile.

19 When the conductive material is aluminum, tungsten, platinum, or iridium, rather
20 than copper, the presence of oxygen is more acceptable during etch of the organic
21 polymeric material, as previously mentioned. The effect of the presence of various
22 halogens depends on the particular metal used. However, even when the conductive
23 material is aluminum, tungsten, platinum, or iridium, oxygen-comprising or halogen
24 etchant species are typically used as additives to increase etch rate or improve etch
25 profile, but are not the principal etchant species for etching of the organic, polymeric
26 material.

27 The preferred etch plasma of the present invention is a hydrogen/nitrogen-based
28 plasma having principally hydrogen-comprising and/or nitrogen-comprising etchant

1 species. In addition, as described above, depending on the materials used in the device
2 fabrication, the concentration of at least one etchant species generated from a source
3 comprising an element selected from the group consisting of oxygen, chlorine, fluorine,
4 and bromine is minimized. To provide a hydrogen/nitrogen-based plasma, the plasma
5 etchant species comprise principally hydrogen, or principally nitrogen, or principally a
6 mixture thereof. To provide these species, the plasma source gas comprises at least one
7 of the materials selected from the group consisting of hydrogen, nitrogen, ammonia and
8 compounds thereof, hydrazine and compounds thereof, hydroazoic acid, and
9 combinations thereof. When the conductive material to be used in the device is not
10 copper, but is instead aluminum, tungsten, platinum, or iridium, the plasma source gas
11 may comprise hydroxylamine or a compound thereof. The most preferred plasma source
12 gas comprises ammonia; or hydrogen and nitrogen; or a combination of ammonia with
13 hydrogen, nitrogen, or both.

14 Other gases which provide essentially non-reactive etchant species, such as argon,
15 helium, neon, krypton, and xenon may be present in varying amounts, by way of
16 example, and not by way of limitation.

17 In particular, when the organic, polymeric material being etched serves as a
18 patterning mask for etch of a copper film, or when the organic, polymeric material being
19 etched is part of a damascene structure which is to be filled with copper, the etch
20 chemistry provides for use of etchant plasma species where the oxygen, fluorine,
21 chlorine, and bromine content is minimized. Preferably, essentially none of the plasma
22 source gas material furnishes reactive species comprising oxygen, fluorine, chlorine, or
23 bromine. When a patterning mask for etch of a copper film is prepared, should these
24 etchant species contact the copper film, the film is oxidized or otherwise corroded. In
25 addition, etchant species which contain oxygen, fluorine, chlorine or bromine leave
26 deposits of etch byproduct on etched contact via and damascene structure surfaces which
27 may cause oxidation and corrosion of copper depositions made over such surfaces.
28 Further, during etching of some organic-comprising materials, oxygen and fluorine

1 etchant species tend to have a detrimental effect on a typical contact via or trench etch
2 profile.

3 When the conductive material is aluminum, tungsten, platinum, or iridium, rather
4 than copper, the presence of oxygen is more acceptable during etch of the organic
5 polymeric material. When the metal fill layer is tungsten, platinum, or iridium, the effect
6 of the presence of fluorine, chlorine and bromine depends on the particular material used,
7 as is known to one skilled in the art. However, even when the conductive material is
8 aluminum, tungsten, platinum or iridium, oxygen-comprising or halogen etchant species
9 are typically used as additives to increase etch rate or improve etch profile, or to control
10 residue on an etch surface, but are not the principal etchant species for etching of the
11 organic, polymeric material.

12 Figure 4A shows a schematic of a cross-sectional view of a test wafer comprising
13 a series of etched contact vias 405 overlying an aluminum layer 408. (In a damascene
14 process or a dual damascene process, aluminum layer 408 would be replaced by a series
15 of lines or other multi-leveled interconnect structures.) Each contact via 405 is created
16 through a multilayered etch stack structure 400, which includes, from top to bottom, a
17 layer of silicon oxide patterned hard mask 402, and a layer of FLARE™ low k dielectric
18 404. Underlying the low k dielectric layer 404 is a layer of titanium nitride 406, and
19 underlying the titanium nitride is a layer of aluminum 408. Due to the etch chemistry
20 used to etch the via, the low k dielectric, a poly(arylene ether), is severely undercut
21 beneath the patterned silicon oxide hard mask.

22 In detail, the multilayer etch stack included: A silicon dioxide layer (TEOS) 402
23 approximately 2,000 Å thick; and a FLARE™ 2.0 low k dielectric layer 404 (a
24 polyarylene ether, available from Allied Signal, Advanced Microelectronic Materials,
25 Sunnyvale, California) approximately 8,000 Å thick. Underlying the low k dielectric
26 layer 404 was an underlying titanium nitride layer 406 approximately 800 Å thick, and
27 underlying that was an aluminum layer 408 approximately 5,000 Å thick. The feature
28 size of the vias was about 0.3 μm and the aspect ratio was about 4 : 1 (including the

1 silicon dioxide layer 402 and the low k dielectric layer 404). The etching processes
2 were carried out in a CENTURA® Metal Etch Integrated Processing System including a
3 decoupled plasma source (DPS), available from Applied Materials, Inc. of Santa Clara,
4 California, under the following set of conditions, which generally provided a high
5 density plasma.

6 The silicon dioxide layer was etched through a patterned 1 μm thick masking
7 layer of DUV photoresist (which is not shown in Figure 4A). The plasma source gas for
8 etching silicon dioxide layer 402 was 100 sccm of argon, 60 sccm of CHF_3 , and 20 sccm
9 of CF_4 . The Source Power was about 2,000 W at a frequency of about 2 MHz; the Bias
10 Power was about 600 W at a frequency of about 13.56 MHz; the substrate support platen
11 (cathode) temperature was about 30 °C; the helium pressure on the backside of the 200
12 mm wafer substrate was about 12 Torr; the process chamber pressure was about 10 mT;
13 the chamber wall temperature was about 80 °C; and the etch time was about 30 seconds.

14 The FLARE™ 2.0 low k dielectric layer 404 was sequentially etched in the same
15 process chamber using a plasma source gas of 60 sccm of oxygen. The Source Power
16 was about 1200 W; the Bias Power was about 400 W; the substrate support platen
17 temperature was about 30 °C; the helium backside pressure was about 7 Torr; the process
18 chamber pressure was about 8 mT; the chamber wall temperature was about 80 °C; and
19 the etch time was about 60 seconds.

20 Figure 4B shows a schematic of a cross-sectional view of the same series of
21 etched contact vias shown in Figure 4A, except that the etch chemistry of the present
22 invention was used to provide nearly straight sidewalls on the etched via.

23 The silicon dioxide layer was etched through a patterned, 1 μm thick masking
24 layer of DUV photoresist (which is not shown in Figure 4B). The plasma source gas for
25 the etching of silicon dioxide layer 422 was 100 sccm of argon, 60 sccm of CHF_3 , and 20
26 sccm of CF_4 . The Source Power was about 2,000 W; the Bias Power was about 600 W;
27 the substrate support platen (cathode) temperature was about 5 °C; the helium pressure
28 on the backside of the 200 mm wafer substrate was about 7 Torr; the process chamber

1 pressure was about 10 mT; the chamber wall temperature was about 80°C; and the etch
2 time was about 30 seconds. Subsequent to this etch step, the etch processing chamber
3 was dry-cleaned using an oxygen plasma, and seasoned by etching unpatterned
4 photoresist in an ammonia (NH₃) plasma.

5 The FLARE™ 2.0 low k dielectric layer 404 was etched using a plasma source
6 gas of 70 sccm of NH₃. The Source Power was about 1800 W; the Bias Power was about
7 300 W; the substrate support platen temperature was about 5 °C; the helium backside
8 pressure was about 16 Torr; the process chamber pressure was about 8.5 mT; the
9 chamber wall temperature was about 80°C; and the etch time was about 140 seconds.

10 When an integrated series of etch steps is carried out in a single process chamber
11 and an etch step produces a fluorine-comprising byproduct, it is advisable to dry clean
12 the process chamber subsequent to that etch step and prior to proceeding to an etch step
13 in which an organic polymeric material is etched. This is particularly important when the
14 feature size of the pattern being etched is 0.25 μm or smaller.

15 In an additional experiment, all etch process conditions were the same as those
16 which produced the straight sidewalls shown in Figure 4B, but there was no dry cleaning
17 of the etch process chamber between the etching of the silicon dioxide layer (using a
18 fluorine-containing etchant species) and the etching of the low k dielectric layer. The
19 etch profile was nearly the same as that shown in Figure 4B, except that the upper
20 surface of the silicon dioxide layer was attached and became faceted. Faceting refers to
21 the corner edges of the hard mask being etched so that they become cut off and the mask
22 opening becomes widened, resulting in a larger upper contact surface area. If the next
23 layer of metal lines is slightly misaligned, this can result in shorting of metal lines in the
24 device. An increased presence in the amount of fluorine byproduct resulted in increased
25 faceting of the hard mask corners.

26 The etch chemistry described above can be used to etch other organic, polymeric
27 layers, and especially low k dielectric materials such as SILK™, an organic polymer
28 similar to BCB (divinylsiloxane bis-benzocyclobutene), which does not contain silicon,

1 available from Dow Chemical Co., Midland Michigan; FLARE 2.0™, a poly(arylene
2 ether) available from Allied Signal Advanced Microelectronic Materials, Sunnyvale,
3 California, which does not contain fluorine, despite its name. Although SILK™, and
4 FLARE 2.0™ have been determined to work well, there are numerous other low k
5 dielectric materials which are expected to behave in a similar manner when etched in
6 accordance with the method of the present invention, using the etch chemistry described
7 herein. Preferably these other low k dielectric materials do not include silicon or
8 fluorine. Other non-fluorine-containing low k dielectrics include poly(arylene)ethers;
9 Poly(arylene)ether oxazoles; Parylene-N; Polyimides; Polynaphthalene-N; Polyphenyl-
10 Quinoxalines (PPQ); Polybenzoxazoles; Polyindane; Polynorborene; Polystyrene;
11 Polyphenyleneoxide; Polyethylene; Polypropylene; and similar materials.

12 A hydrocarbon-based plasma of the kind previously described can be used to etch
13 organic polymeric layers in the manner described above. In one preferred embodiment,
14 the principal plasma source gas is methane (CH₄). However, typically the methane is
15 used in combination with ammonia, hydrogen, nitrogen, or a combination thereof.
16 Chemically inert gases may be used as diluents. The volumetric flow rate of the source
17 gas for the principal etchant species is in the range of about 50 - 100 sccm, with additive
18 etchant species source gases, if any, being present in lesser amounts. Overall etch
19 process variables are in the same ranges as those provided above for a hydrogen/nitrogen
20 plasma in the CENTURA ® METAL ETCH, DPS processing system.

21 In conclusion, the use of new (other than aluminum) conductive materials such as
22 copper, platinum and iridium, in combination with high dielectric constant materials such
23 as barium strontium titanate, and low dielectric constant materials such as FLARE ® and
24 SILK ®, permits the continuing down scaling of integrated circuit devices and systems
25 while providing improved performance. In addition use of such materials enables
26 reduced power consumption as well as new device functionality. The methods of the
27 present invention make it possible to take advantage of these new materials.

28 The above described preferred embodiments are not intended to limit the scope

1 of the present invention, as one skilled in the art can, in view of the present disclosure
2 expand such embodiments to correspond with the subject matter of the invention claimed
3 below.

CLAIMS

We claim:

- 1 1. A method for patterning semiconductor device features comprising the steps of:
2 (a) transferring a pattern from a patterned photoresist layer through a layer of
3 high-temperature inorganic masking material;
4 (b) transferring the pattern from a multi-layered structure remaining after step (a)
5 through an underlying layer of a high-temperature organic-based masking material;
6 (c) removing any photoresist material which remains after step (b); and
7 (d) transferring the pattern from the multi-layered structure present after step (c)
8 through a feature layer underlying said high-temperature organic-based masking
9 material, wherein said feature layer comprises aluminum.
- 1 2. A method for patterning semiconductor device features comprising the steps of:
2 (a) transferring a pattern from a patterned photoresist layer through a layer of
3 high-temperature inorganic masking material;
4 (b) transferring the pattern from a multi-layered structure remaining after step (a)
5 through an underlying layer of a high-temperature organic-based masking material which
6 is a low k dielectric; and
7 (c) removing any photoresist material which remains after step (b);
- 1 3. The method of Claim 2, wherein said high-temperature organic-based masking
2 material which is a low k dielectric is a plasma-deposited material.
- 1 4. The method of Claim 3, wherein said plasma-deposited low k dielectric material is

2 selected from the group consisting of Poly(arylene)ethers, Poly(arylene)ether oxazoles,
3 Parylene-N, Polyimides, Polynaphthalene-N, Polyphenyl-Quinoxalines,
4 Polybenzoxazoles, Polyindane, Polynorborene, Polystyrene, Polyphenyleneoxide,
5 Polyethylene, Polypropylene, α C and combinations thereof.

1 5. A method for patterning semiconductor device features comprising the steps of:

2 (a) developing an imaged layer of high-temperature imageable material into a
3 pattern using a plasma etching technique, to produce a patterned mask which can be used
4 to transfer a desired pattern through underlying layers;

5 (b) transferring the pattern formed in step a) through an underlying layer of high-
6 temperature organic-based masking material; and

7 (c) transferring the pattern from the multi-layered structure present after step (b)
8 through at least one aluminum-comprising feature layer underlying said high-temperature
9 organic-based masking material.

1 6. A mask stack for etching a semiconductor feature, said mask stack comprising:

2 (a) a layer of a low-temperature imageable material;

3 (b) a layer of a high-temperature inorganic material underlying said low-
4 temperature imageable material; and

5 (c) a layer of a high-temperature organic-based material underlying said high-
6 temperature inorganic material, wherein said high-temperature organic-based material is
7 a low k dielectric.

1 7. The mask stack of Claim 6, wherein said low k dielectric is selected from the group
2 consisting of Poly(arylene)ethers, Poly(arylene)ether oxazoles, Parylene-N, Polyimides,
3 Polynaphthalene-N, Polyphenyl-Quinoxalines, Polybenzoxazoles, Polyindane,
4 Polynorborene, Polystyrene, Polyphenyleneoxide, Polyethylene, Polypropylene, α C, and
5 combinations thereof.

1 8. A mask stack for etching a semiconductor feature, said mask stack comprising:
2 (a) a layer of a high-temperature imageable material; and
3 (b) a layer of a high-temperature organic-based material underlying said high-
4 temperature imageable material, wherein said high-temperature organic-based material is
5 a low k dielectric.

1 9. The mask stack of Claim 8, wherein said low k dielectric material is selected from the
2 group consisting of Poly(arylene)ethers, Poly(arylene)ether oxazoles, Parylene-N,
3 Polyimides, Polynaphthalene-N, Polyphenyl-Quinoxalines, Polybenzoxazoles,
4 Polyindane, Polynorborene, Polystyrene, Polyphenyleneoxide, Polyethylene,
5 Polypropylene, α C, and combinations thereof.

1 10. A method for patterning semiconductor device features comprising the steps of:
2 (a) developing an imaged layer of high-temperature imageable material into a
3 pattern using a plasma etching technique, to produce a patterned mask which can be used
4 to transfer a desired pattern through underlying layers;
5 (b) transferring the pattern formed in step a) through an underlying layer of high-
6 temperature organic-based masking material;
7 (c) transferring the pattern from the multi-layered structure present after step (b)
8 through at least one feature layer underlying said high-temperature organic-based
9 masking material;
10 (d) removing residual high-temperature organic-based masking layer material
11 from a surface of said feature layer; and
12 (e) applying a layer of an organic-based material having a dielectric constant
13 which is advantageous for purposes of increasing the gate speed of a transistor, wherein
14 said organic-based dielectric layer comprises a material selected from the group
15 consisting of Poly(arylene)ethers, Poly(arylene)ether oxazoles, Parylene-N, Polyimides,

16 Polynaphthalene-N, Polyphenyl-Quinoxalines, Polybenzoxazoles, Polyindane,
17 Polynorborene, Polystyrene, Polyphenyleneoxide, Polyethylene, Polypropylene, α C, and
18 combinations thereof.

1 11. A method of pattern etching an organic polymeric layer, comprising the steps of:

2 (a) providing a layer of an organic polymeric material having on its surface a
3 patterned material which serves as a mask for purposes of pattern transfer; and

4 (b) contacting said organic polymeric layer with an etchant plasma which is
5 principally a hydrogen/nitrogen-based plasma.

1 12. The method of Claim 11, wherein said etchant plasma contains essentially no
2 oxygen-comprising, fluorine-comprising, chlorine-comprising or bromine-comprising
3 species.

1 13. The method of Claim 11, wherein a source gas used to produce said
2 hydrogen/nitrogen-based plasma comprises ammonia, or hydrogen, or nitrogen, or a
3 combination thereof.

1 14. The method of Claim 13, wherein said hydrogen/nitrogen-based gas includes a non-
2 reactive etchant species.

1 15. The method of Claim 11, wherein said etchant plasma source gas includes an
2 additive material which is used to control etch profile or to control residue at an etch
3 surface.

1 16. The method of Claim 11, wherein said pattern transferred is one useful in a
2 damascene or dual damascene structure.

- 1 17. The method of Claim 13, wherein said pattern transferred is one useful in a
2 damascene or dual damascene structure.
- 1 18. The method of Claim 14, wherein said non-reactive etchant species is selected from
2 the group consisting of argon, helium, neon, krypton, and xenon.
- 1 19. The method of Claim 12, wherein said hydrogen/nitrogen-based plasma is a high
2 density plasma.
- 1 20. A method of pattern etching an organic polymeric layer, comprising the steps of:
2 (a) providing a layer of an organic polymeric material having on its surface a
3 patterned material which serves as a mask for purposes of pattern transfer; and
4 (b) contacting said organic polymeric layer with an etchant plasma which is
5 principally a hydrocarbon-based plasma.
- 1 21. The method of Claim 20, wherein said etchant plasma contains essentially no
2 oxygen-comprising, fluorine-comprising, chlorine-comprising or bromine-comprising
3 species.
- 1 22. The method of Claim 21, wherein a source gas used to produce said hydrocarbon-
2 based plasma is methane.
- 1 23. The method of Claim 22, wherein said hydrogen/nitrogen-based gas includes a non-
2 reactive etchant species.
- 1 24. The method of Claim 20, wherein said pattern transferred is one useful in a
2 damascene or dual damascene structure.

1 25. The method of Claim 21, wherein said pattern transferred is one useful in a
2 damascene or dual damascene structure.

1 26. The method of Claim 22, wherein said pattern transferred is one useful in a
2 damascene or dual damascene structure.

1 27. The method of Claim 23, wherein said non-reactive etchant species is selected from
2 the group consisting of argon, helium, neon, krypton, and xenon.

1 28. The method of Claim 20, wherein said hydrocarbon-based plasma is a high density
2 plasma.

1 29. A method of pattern etching a low k dielectric layer, comprising the steps of:
2 (a) providing a layer of a low k dielectric material having on its surface a
3 patterned material which serves as a mask for purposes of pattern transfer; and
4 (b) contacting said low k dielectric layer with an etchant plasma which is
5 principally a hydrogen/nitrogen-based plasma.

1 30. The method of Claim 29, wherein said low k dielectric material is selected from
2 the group consisting of Poly(arylene)ethers, Poly(arylene)ether oxazoles, Poly(arylene)-N,
3 Polyimides, Polynaphthalene-N, Polyphenyl-Quinoxalines, Polybenzoxazoles,
4 Polyindane, Polynorborene, Polystyrene, Polyphenyleneoxide, Polyethylene,
5 Polypropylene, α C, and combinations thereof.

1 31. The method of Claim 30 or Claim 31, wherein said etchant plasma contains
2 essentially no oxygen-comprising, fluorine-comprising, chlorine-comprising, or bromine-
3 comprising species.

1 32. The method of Claim 31, wherein said hydrogen/nitrogen-based plasma is a high
2 density plasma.

1 33. The method of Claim 29 or Claim 30, wherein said hydrogen/nitrogen-based
2 plasma is generated from a source gas which comprises ammonia, or hydrogen, or
3 nitrogen, or a combination thereof.

1 34. The method of Claim 33, wherein said source gas includes a non-reactive etchant
2 species.

1 35. The method of Claim 34, wherein said non-reactive etchant species is selected
2 from the group consisting of argon, helium, neon, krypton, and xenon.

1 36. The method of Claim 29 or Claim 30, wherein said etchant plasma is generated
2 from a source gas which includes an additive material which is used to control etch
3 profile or to control residue at an etch surface.

1 37. The method of Claim 29 or Claim 30, wherein said pattern transferred is one
2 useful in a damascene or dual damascene structure.

1 38. A method of pattern etching a low k dielectric layer, comprising the steps of:
2 (a) providing a layer of a low k dielectric material having on its surface a
3 patterned material which serves as a mask for purposes of pattern transfer; and
4 (b) contacting said low k dielectric layer with an etchant plasma which is
5 principally a hydrocarbon-based plasma.

1 39. The method of Claim 38, wherein said low k dielectric material is selected from
2 the group consisting of Poly(arylene)ethers, Poly(arylene)ether oxazoles, Parylene-N,

3 Polyimides, Polynaphthalene-N, Polyphenyl-Quinoxalines, Polybenzoxazoles,
4 Polyindane, Polynorborene, Polystyrene, Polyphenyleneoxide, Polyethylene,
5 Polypropylene, α C, and combinations thereof.

1 40. The method of Claim 38 or Claim 39, wherein said etchant plasma contains
2 essentially no oxygen-comprising, fluorine-comprising, chlorine-comprising, or bromine-
3 comprising species.

1 41. The method of Claim 40, wherein a source gas used to produce said hydrocarbon-
2 based plasma is methane.

1 42. The method of Claim 41, wherein said source gas includes a non-reactive etchant
2 species.

1 43. The method of Claim 42, wherein said non-reactive etchant species is selected
2 from the group consisting of argon, helium, neon, krypton, and xenon.

1 44. The method of Claim 40, wherein said hydrocarbon-based plasma is a high
2 density plasma.

1 45. The method of Claim 29 or Claim 30, wherein said pattern transferred is one
2 useful in a damascene or dual damascene structure.

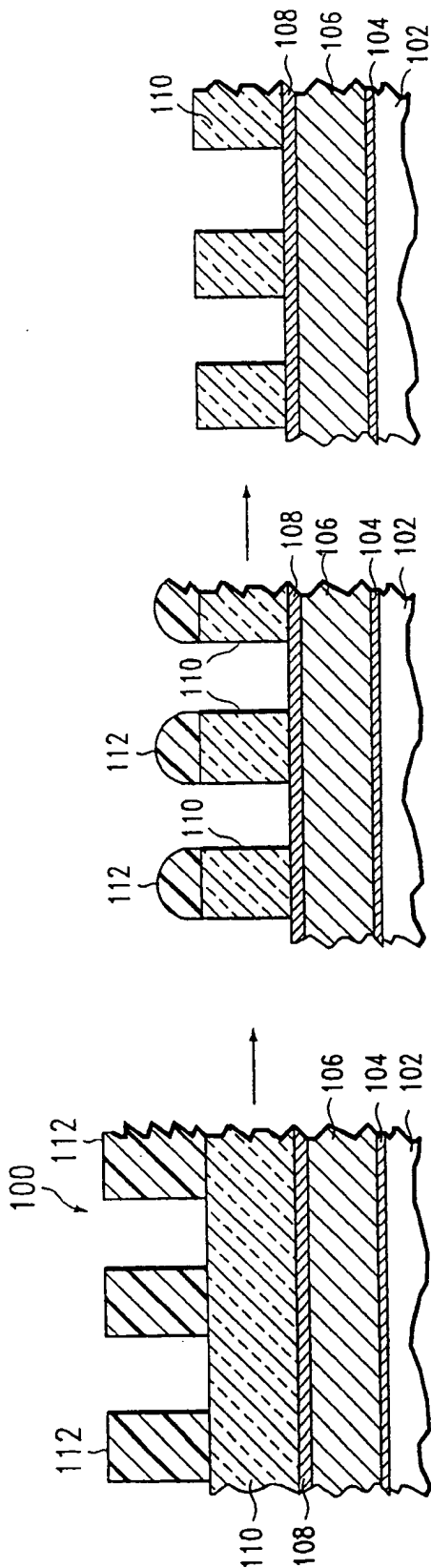


FIG. 1C (PRIOR ART)

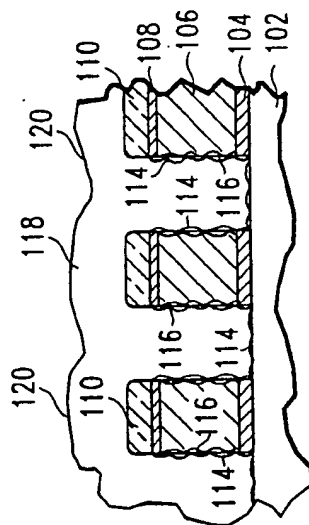


FIG. 1E (PRIOR ART)

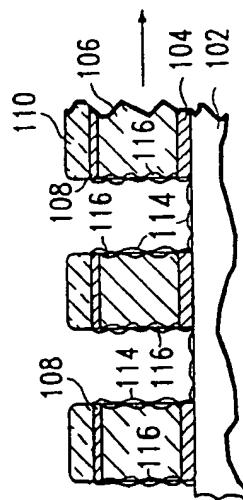


FIG. 1D (PRIOR ART)

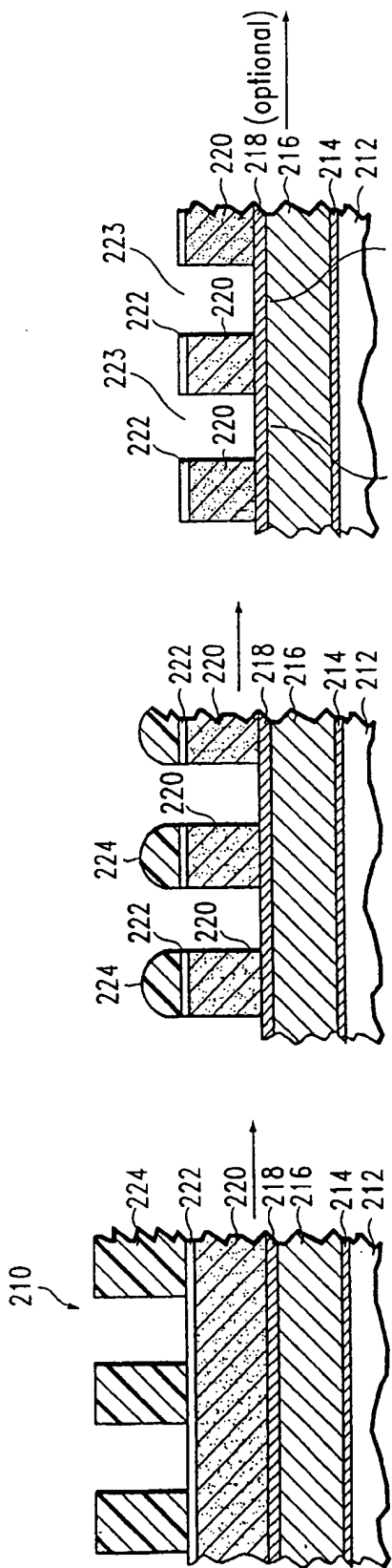


FIG. 2A

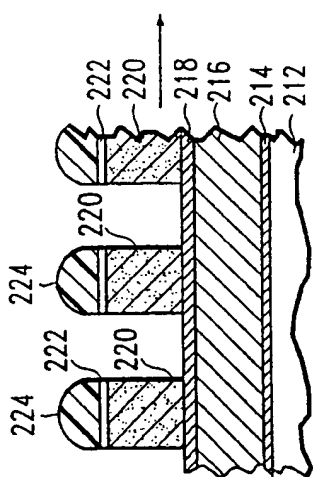


FIG. 2B

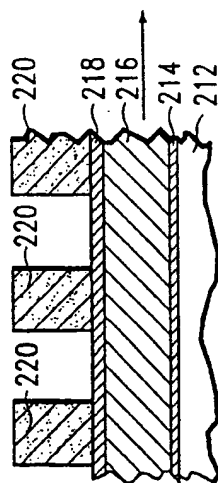


FIG. 2D
(Optional)

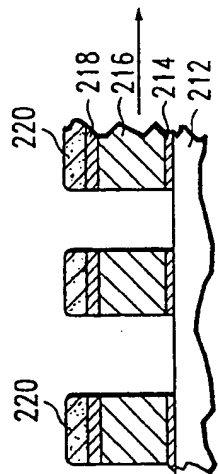


FIG. 2E

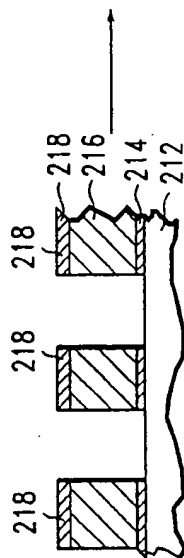


FIG. 2F

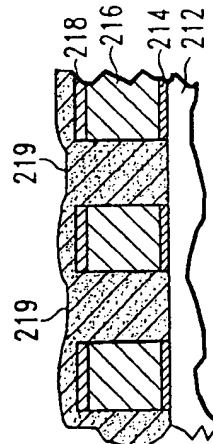


FIG. 2G

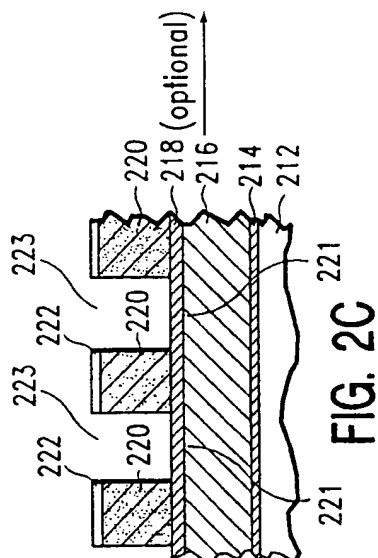


FIG. 2C

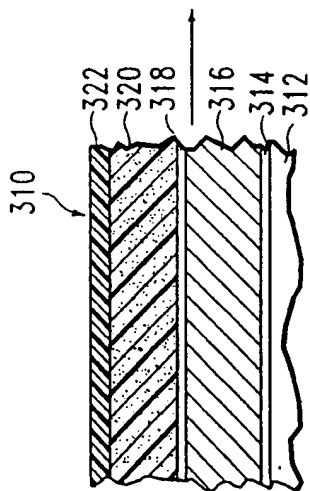


FIG. 3A

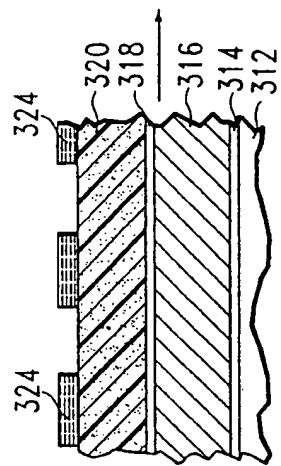


FIG. 3C

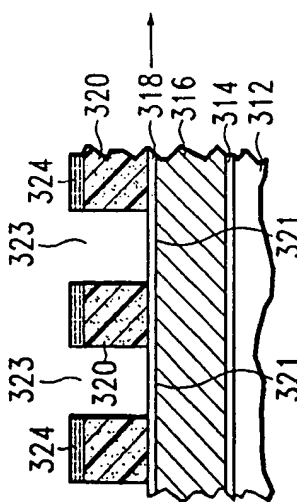


FIG. 3D

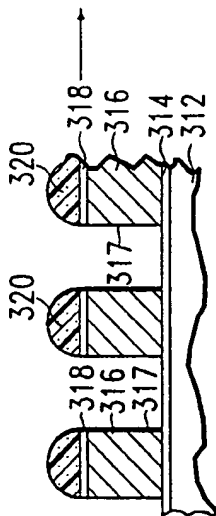


FIG. 3E

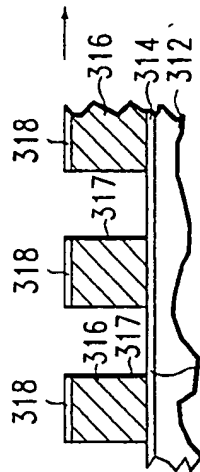


FIG. 3F

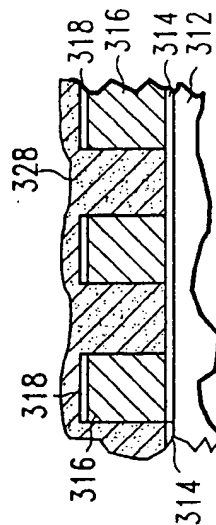


FIG. 3G

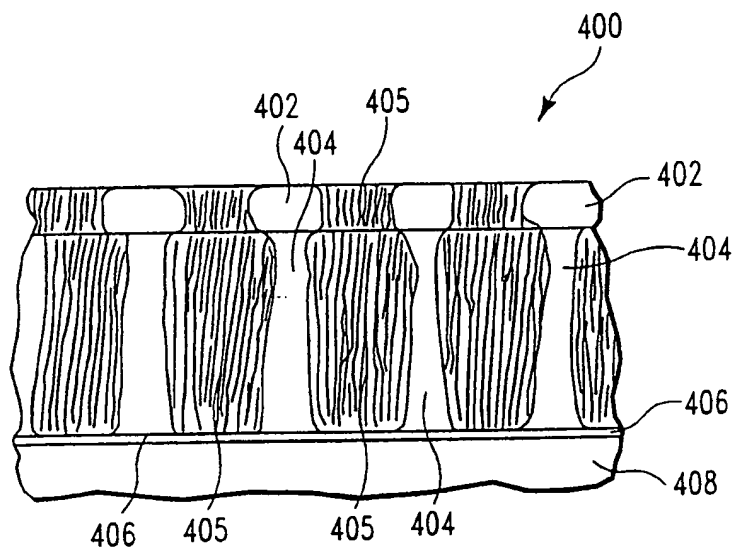


FIG. 4A

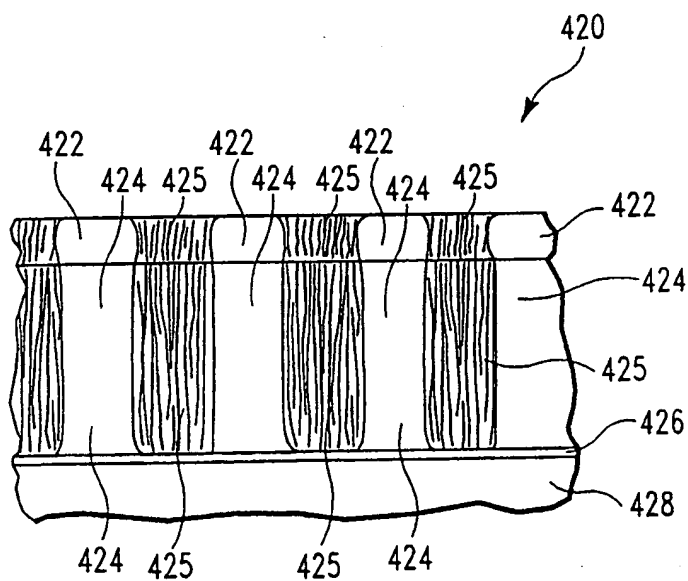


FIG. 4B

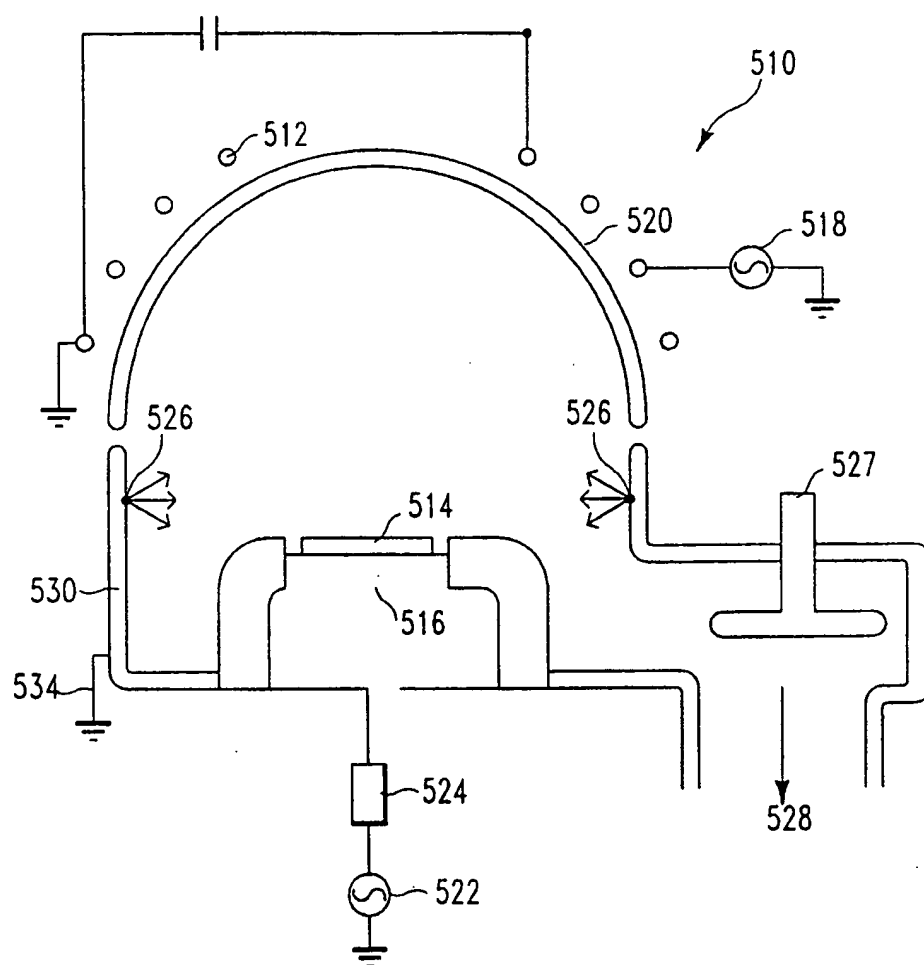


FIG. 5 (PRIOR ART)

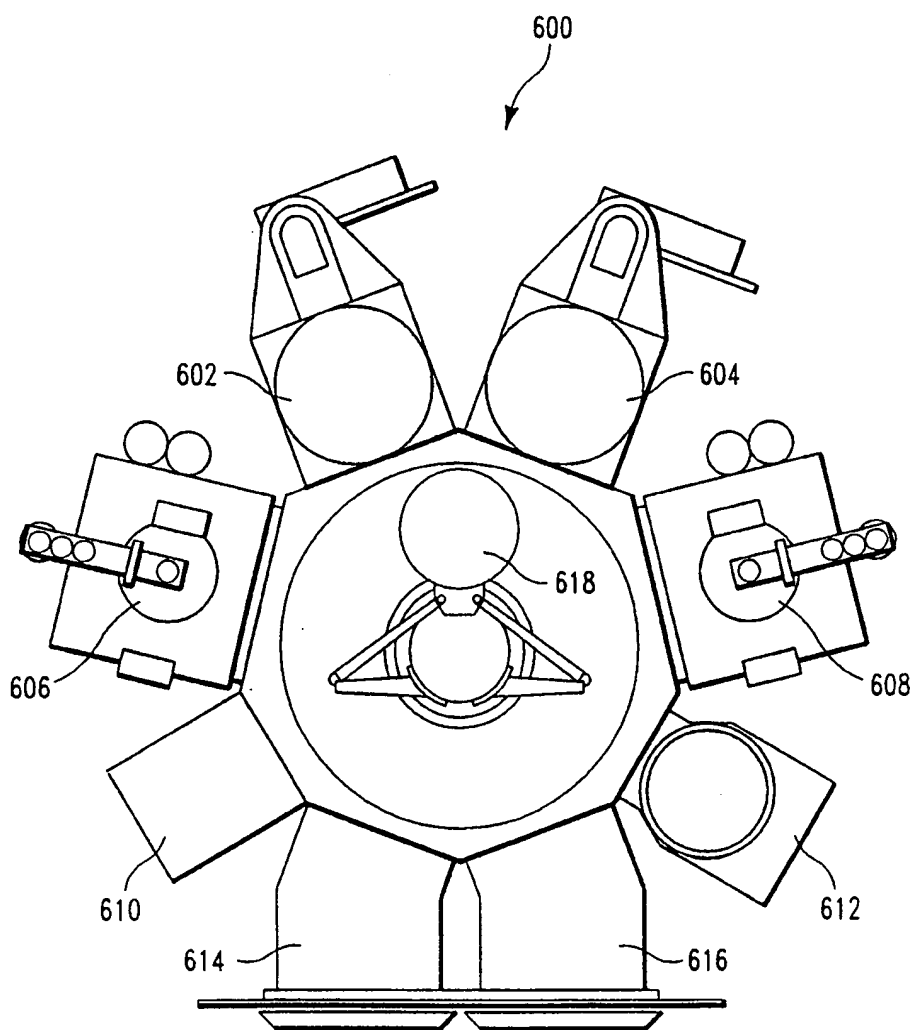


FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 99/23597

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/311

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 296 707 A (HEWLETT PACKARD CO) 28 December 1988 (1988-12-28) column 3 -column 5 ---	
A	US 4 528 066 A (STANASOLOVICH DAVID ET AL) 9 July 1985 (1985-07-09) column 5, line 59 - line 66 column 7, line 1 - line 5 ---	
A	US 5 230 772 A (KADOMURA SHINGO) 27 July 1993 (1993-07-27) column 2, line 36 - line 60 --- -/--	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

7 February 2000

Date of mailing of the international search report

08. 03. 2000

Name and mailing address of the ISA

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Fax: (+31-70) 340-3016

Authorized officer

Szarowski, A

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	BAKLANOV M R, VANHAELEMEERSCH S, ALAERTS C, MAEX K: "Plasma etching of organic low-dielectric- constant polymers: comparative analysis" MATER. RES. SOC. SYMP. PROC. , vol. 511, 1998, pages 247-252, XP000874697 Low-dielectric constant materials IV. symposium, San Francisco, CA, USA, 14-16 april 1998 -----	
A	US 5 346 586 A (KELLER DAVID J) 13 September 1994 (1994-09-13) column 4, line 62 - line 66 -----	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 99/23597

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: all
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims Nos.: all

All the claims relate to an extremely large number of possible methods. Support within the meaning of Art. 6 PCT and disclosure within the meaning of Art. 5 PCT is to be found only for a very limited number of methods. Furthermore the large number of independent claims, with partially overlapping scope is such that a lack of clarity and conciseness within the meaning of Article 6 PCT arises to such an extent as to render a meaningful search of the claims impossible.

Consequently, the search has been carried out for those parts of the application which do appear to be clear and concise, namely the search was limited to the example described p36-37, fig 4b of the application.

The searched claim was:

A method of patterning a polyarylene ether layer comprising the steps of:

- 1- providing a silicon oxide layer on top of the polyarylene ether
- and
- 2- etching the silicon oxide layer in a plasma comprising CHF₃ and CF₄
- 3- etching the polyarylene ether layer in a plasma comprising NH₃.

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 99/23597

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0296707 A	28-12-1988	JP 2021640 A US 5110712 A	24-01-1990 05-05-1992
US 4528066 A	09-07-1985	EP 0167136 A JP 1824683 C JP 5033530 B JP 61026225 A	08-01-1986 10-02-1994 19-05-1993 05-02-1986
US 5230772 A	27-07-1993	JP 4084414 A	17-03-1992
US 5346586 A	13-09-1994	NONE	